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BY
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Lifetime Prediction of the Boost, Z-source and Y-source Converters in a Fuel Cell Hybrid Electric Vehicle Application

by

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Brwene Gadalla

July, 2017
Aalborg Øst, Denmark

English Abstract

Reliability is one of the most important issues in the field of power electronics components and systems. In most of the electro-mobile applications, e.g. electric and hybrid electric vehicles, power electronic are commonly used in a very harsh environment. Temperature variations, thermal cycles, power cycles, humidity, vibration and other stresses affecting the device may cause unreliable systems. Thus, designing reliable power electronic converters is important for the aim of reducing the energy losses, maintenance cost and extending the service lifetime as well. Research within power electronics is of high interest as it has a huge impact in the industry of the electro-mobile applications.

Boost converters are essentially needed in many applications such as electro-mobility, fuel cell, and renewable energy applications that require the output voltage to be higher than the input voltage. Recently, boost type converters have been attracted by the industrial applications, and hence it has become an extremely hot topic of research. Many researchers have proposed the impedance source converters with their unique advantages as having a high voltage gain in a small range of duty cycle ratios. However, the thermal behaviour of the semiconductor devices and passive elements in the impedance source converter is an important issue from a reliability point of view and has not been investigated yet in impedance source converters. Therefore, a loss distribution comparison between three different types (Conventional boost, Z-source and Y-source) of the boost converters has been analysed for a wide voltage and power range. The Y-source converter has been selected for validating the influence of heat loss generated from the devices. A simulation model is developed and verified experimentally by a 300 W prototype Y-source converter.

Fuel cells are a very promising technology since they are pollution free, producing only electricity, water, and heat. There has been a significant force

in the development of the fuel cell technology over the past 30 years, and is drawing an increasing attention towards the technology today. Fuel cells have been applied to DC/DC converters where the reliability and lifetime are of high priority. A lifetime prediction model is applied for the power semiconductors, which are used in the fuel cell DC/DC converters. The common used Coffin- Manson lifetime model and Semikron lifetime model for the IGBTs solder and bond wire fatigues are considered and compared in the three DC/DC converters. In order to estimate the lifetime of the converters, a mission profile is taken into account to estimate the impact of the IGBTs junction temperature and thus the lifetime during the steady state operation. In addition to the thermal stresses generated due to the power losses during the converter operation, a case study of Artemis motorway driving cycle is considered in this analysis. Lifetime consumption and the expected number of years before failure is presented and compared for the Boost, Z-source and Y-source converters. The lifetime estimation results show that the Z-source converter has a longer lifetime compared with the conventional boost and Y-source converter, due to lowest maximum junction temperature profile of the Z-source converter. Nevertheless, each converter is designed separately according to its current and voltage stresses of the power device, where both the Z-source and Y-source converters have IGBT modules with the same power rating.

This Ph.D. thesis starts with the state of the art of the reliability of power electronics in the electro-mobile applications, and the Fuel Cell Hybrid Electric Vehicle (FCHEV) system configuration. The design, parameter selection, and basic theory of operation of the boost (conventional, Z-source and Y-source) power converters are discussed in Chapter 2. In Chapter 3 the loss and temperature modelling are given at different power loading. Chapter 4 analyzes the three compared converters at different voltage and power levels, and validate the loss modelling of the Y-source converter based on the temperature modelling. The reliability assessment for three converters is given in Chapter 5, where the lifetime modelling, failures mechanisms, and the number of estimated lifetime years of the converters are presented based on the assessment of only one component, which is the IGBT power module.

Finally, in Chapter 6 the conclusions, main contributions, and future work is given to give a full overview of this Ph.D. project.

Dansk Resumé

Pålidelighed er et af de vigtigste spørgsmål inden for effektelektroniske komponenter og systemer. I de fleste elektro-mobile applikationer, f.eks. elektriske og hybrid elektriske køretøjer, er effektelektronikken anvendt i et meget hårdt miljø. Temperaturvariationer, termiske kredsløb, lastcykluser, vibrationer og andre påvirkninger, der påvirker enheden, kan forårsage upålidelige systemer. Således er design af pålidelige effektelektroniske omformere vigtigt for at reducere energitab, vedligeholdelsesomkostninger og forlænge servicetiden også. Forskning inden for effektelektronik er af stor interesse, da den har en stor indflydelse i industrien indenfor elektro-mobile applikationer.

Boost-omformere er nødvendige i mange applikationer såsom elektromobilitet, brændselsceller og vedvarende energi applikationer, der kræver, at udgangsspændingen er højere end indgangsspændingen. Mange forskere foreslog "impedans-source" omformere med deres unikke fordele som at have en høj spændingsforstærkning med en lille "duty cycle". De termiske egenskaber for de aktive og passive elementer i "impedanse-source" omformeren er imidlertid et vigtigt problem ud fra et pålidelighedssynspunkt og er endnu ikke undersøgt. Derfor er en tabsfordelingssammenligning mellem tre forskellige typer (Konventionelle boost, Z-source og Y-source) af boost-omformerne blevet analyseret for et bredt spændings- og effektområde. Y-source omformeren er valgt til at validere indflydelsen af varmetab, der genereres fra enhederne. En simuleringsmodel er udviklet og verificeret eksperimentelt med en 300 W prototype Y-source omformer.

Brændselsceller er en meget lovende teknologi, da de er forureningsfrie og kun producerer elektricitet, vand og varme. Det har undergået en væsentlig teknologisk udvikling sidste 30 år og der tegner sig en stigende opmærksomhed mod teknologien i dag. Brændselsceller er blevet anvendt til DC / DC-omformere, hvor pålideligheden og levetiden er af høj prioritet. Der anvendes en levetidsprognosemodel for halvledere, som anvendes i DC /

DC-omformere til brændselsceller. Den fælles brugte Coffin- Manson levetidsmodel og Semikron levetidsmodel til IGBT'ens loddemetal og udmattelse af trådlodning vurderes og sammenlignes i de tre DC / DC-omformere. For at vurdere omformernes levetid tages der hensyn til en lastprofil for at vurdere virkningen af IGBT'ens forbindelsestemperatur og dermed levetiden under stabil drift. Ud over de termiske spændinger, der genereres på grund af strømforbruget under brug, et konkret eksempel med Artemis motorvejskørecyklus anvendt i denne analyse. Levetidsforbrug og det forventede antal år før fejl præsenteres og sammenlignes for Boost, Z-source og Y-source omformere. Resultatet af levetidsopgørelsen viser, at Z-source- omformeren har en længere levetid sammenlignet med den konventionelle boost- og Y-source-omformer på grund af den laveste maksimale forbindelsestemperatur for Z-source- omformeren. Hver omformer er designet separat afhængigt af strømforsyningens levetidssammenligningen, hvor både Z-source og Y-source omformere har IGBT moduler med samme effekt klassificering.

Denne Ph.D. afhandling begynder med at præsentere den nyeste viden om pålidelighed af effektelektroniske omformere i elektro-mobile applikationer. FCHEV-systemets konfiguration præsenteres. Udformningen, parametervalg og grundlæggende teori om virkemåden af boost (konventionelle, Z-source og Y-source) -omformere omtales i kapitel 2. I kapitel 3 er tabsmodellering og temperaturmodellering givet ved forskellige strømbelastninger. Kapitel 4 analyserer de tre sammenlignede omformere ved forskellige spændings- og effektniveauer, og tabsmodelleringen af Y-source-konverteren valideres baseret på temperaturmodelleringen. Pålidelighedsvurderingen for de omformere er angivet i kapitel 5, hvor levetidsmodellering, fejlmekanismer og antallet af levetidsår af omformerne præsenteres ud fra vurderingen af kun en komponent, som er IGBT-effektmodulet.

I kapitel 6 præsenteres konklusionerne, hovedbidragene og det fremtidige arbejde.

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Report

Chapter. 1

Introduction

In this chapter, an overview of the state of the art in reliability egineering of power electronics in electro-mobile applications is given. This given overview is one of the contributions in this PhD project and it is a partially direct copy from my paper [1] which is published during my PhD study with the following details:

[1] B. Gadalla, E. Schaltz, and F. Blaabjerg, "A survey on the reliability of power electronics in electro-mobility applications," in Intl Conference on Optimization of Electrical Electronic Equipment (OPTIM), Sept 2015, pp. 304–310.

1.1 Introduction

This chapter presents the background of reliability engineering of power electronics used in electro-mobile applications. It includes a state of the art of reliability in power electronics, sources of failure, components failure and different life time prediction methods. Moreover, a general description of the system configuration of the fuel cell hybrid electric vehicle (FCHEV) and the driving cycle used. Then, the thesis structure is presented to give a better understanding about the flow of this research work. All the publications related to this project are listed at the end of the thesis.

1.2 Project background

This Ph.D. project presents a background of the boost power converters, which are used in many applications. A comparison has been made between three existing types of boost power converters (Conventional Boost, Z-source and Y-source).

These types of boost converters are essentially needed in many applications [2] as also discussed later in Chapter 2. A better understanding of their thermal aspects is important for their design in order to obtain a robust system. Therefore, it is of high interest to investigate and compare their thermal performances, which have an indirect impact on the reliability and the efficiency [3], [4].

Power converters are being used in many different applications like industrial motor drives [5, 6] renewable generation systems [7] and more recently also electric vehicles [8, 9]. In order to have design flexibility, power converters should have both voltage-buck and boost capabilities. For that, many new topologies have been proposed with each being claimed to have impressive advantages as for example, the capability of ideally giving an infinite output voltage regardless of the input voltage, using relatively small duty cycle ratios for boosting the voltage which may improve the power losses generated from the devices ect. [10, 11]. These advantages are, without doubt, verified in the laboratories by researchers, but at present, a collective investigation of some of the existing boost converters has not been initiated especially with reference to their thermal and reliability properties. As an example of these existing boost converters, two topologies of the impedance-source converters are selected to initiate this investigation [2].

For illustrating its operational principles, the examples of Boost converter, Z-source converter (ZSC) [12] and Y-source converter (YSC) [13] shown in Fig. 1.1 (a), (b), and (c) are chosen as a firm base for beginning with the investigation. The ZSC and YSC have the capability of ideally giving an infinite output voltage regardless of the input voltage. This boosting feature has so far been recommended for different applications including photovoltaic (PV), electric vehicles (EV), wind power generators, battery management system (BMS).

The Boost converter circuit, which is shown in Fig.1.1 (a) and it compromises one active switch SW, a diode D_1, an inductor L_1, and a capacitor C_1 for introducing a high voltage boost. The Z-source converter circuit is shown Fig.1.1 (b). It consists of two inductors (L_1, L_2) and two capacitors (C_1, C_2) connected in an 'X' shape to be coupled to the dc voltage source.

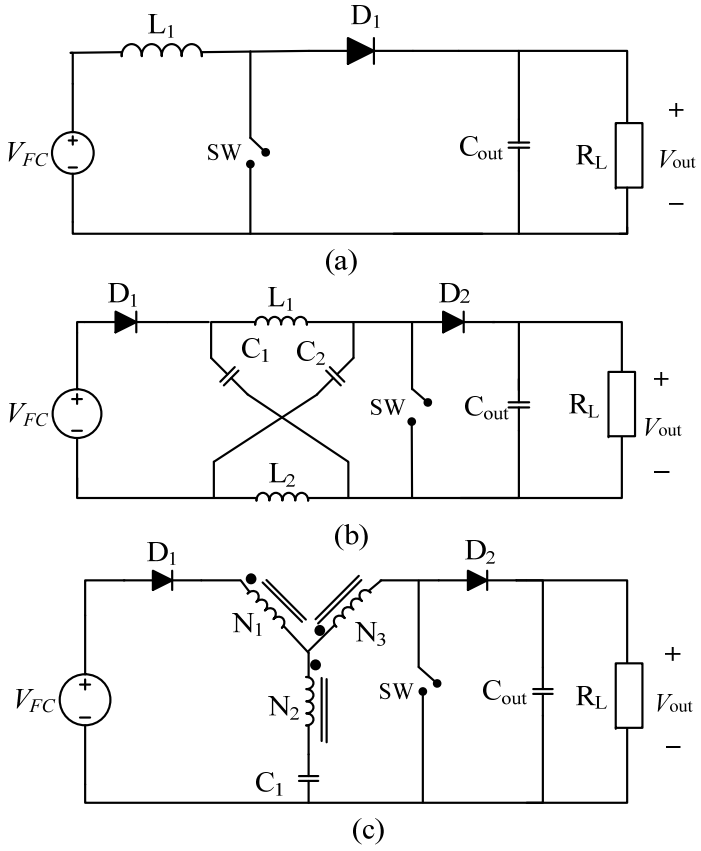


Fig. 1.1: Impedance source converters. a) Boost converter equivalent circuit. b) Z-Source converter equivalent circuit. c) Y-Source converter equivalent circuit [2].

The Y-source impedance network converter and its two modes of operation are shown Fig.1.1 (c). It is realized by a three-winding coupled inductor (N_1, N_2, and N_3) for introducing the high boost at a small duty ratio for the SW. It has an active switch SW, two diodes (D_1, D_2), a capacitor C_1, and the windings of the coupled inductor are connected directly to SW and D_1, to ensure a very small leakage inductance at its winding terminals [2].

It is therefore conceptually logical to describe a particular application which in this case, is a fuel cell hybrid electric vehicles (FCHEV). The discussion will mainly be direct through the reasons for selecting that particular application by stating their advantages and disadvantages, and the reliability

aspects of an FCHEV configuration.

1.3 System configuration of FCHEV and Driving cycle

"Electric vehicle" is an extensive expression, which can be used to describe different types and sizes of trucks and cars. These types could be one of the following; plug-in electric, hybrid-electric, and battery electric vehicles. In addition, fuel cell technologies could be also considered [14], [15] as the source of power.

One of the main advantages of Fuel Cell Vehicles (FCVs) is the usage of oxygen and hydrogen extracted from the sources of renewable energy [16]. Therefore, FCVs are considered as a clean source, and hence, categorized as "*zero-emission vehicles*" [17]. The fuel cells are characterized by giving DC output voltage, but this voltage is only constant if the operating conditions are also constant [18].

In Fig 1.2 a system configuration of fuel cell hybrid electric vehicles (FCHEV) [19] is shown, which consists of a fuel cell stack, DC/DC converter, auxiliary devices, inverter and motor. The fuel cell stack delivers the power to the wheels [20]. The torque of the wheels are provided by a differential in order to compensate the speed difference between the high speed of the electric machine shaft and the lower speed of the wheels.

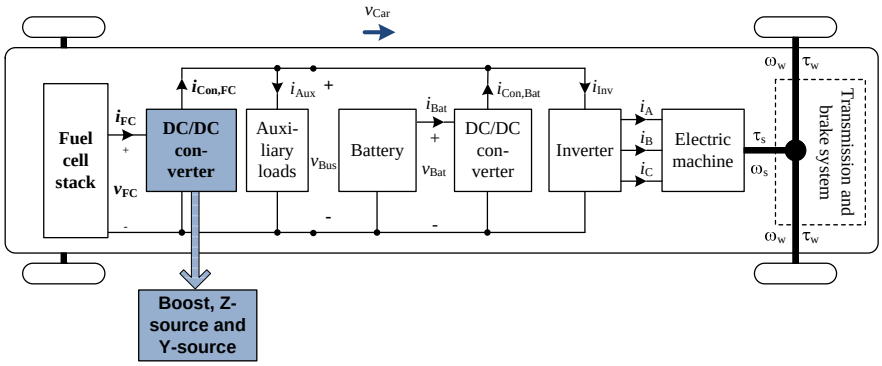


Fig. 1.2: Fuel cell hybrid electric vehicle configuration [19]

The torque and the speed of machine are controlled by the inverter where it inverts the DC voltage of the battery to a three phase AC voltage which is

usfel for the electric machine. Transferring the power from the low voltage side (fuel cell stack) to the high voltage side of the battery is possible through the DC/DC converter [19].

Furthermore, the assessment of the three converter topologies (Boost, Z-source and Y-source) are shown in Fig 1.2 is based on the same FCHEV application and the same input driving cycle.

Driving cycle: The speed characteristics of FCEVs is necessary when designing the power system of the hybrid electric vehicle model. The speed and power characteristics of the fuel cell converter are often obtained by setting up models of the vehicles these models are based on the loads acting on the vehicles [19]. Further a description of the system configuration and the driving cycle is given in Chapter 5.

The advantages of the FCHEV are [21]:

1) Fuel Efficient - The hydrogen fuel cell powered vehicles fuel consumption are equivalent to about half of the gasoline powered vehicles. Fuel cell vehicles are often equipped with regenerative brakes, which also contribute to their increased efficiency [22].

2) Reduced Pollution - Since the hydrogen cars only emits heat and water and it can be powered from renewable energy, which therefore is a clean source [22].

3) Reduced Maintenance - Lesser internal moving parts means lower maintenance related costs. Hydrogen powered vehicles are more quiet, and normally more light in weight [23].

4) Uni-directional power flow - The FCHEV requires only uni-directional power flow un-like a battery converter, which requires bi-directional power flow.

5) Fast Refuelling - Although the amount of fill up stations are limited, filling up a hydrogen car takes only a few minutes with enough fuel to travel several hundred miles in contrast to pure battery electric vehicles [24].

Disadvantages of the FCHEV [21]:

1) Lacking Infrastructure - Currently there is a lacking sufficient infrastructure to support hydrogen refuelling on a mass scale [25].

2) Potential Dangers - One of the main concerns is that Hydrogen combustions are almost unseen [26]. Storing pressurized hydrogen on board, the vehicle can pose unique dangers.

3) Hydrogen Storage - In order to store Hydrogen a chemical procedure is needed to be stored efficiently [27].

4) Climate Sensitivity - The Hydrogen power-driven cars are having some temperature restrictions. It includes both risks, fuel cell water freezing and overheating of the fuel cell components depending on the weather conditions [28], [29].

5) Vehicle Production Costs - Platinum is one of the expensive materials, which is frequently used for fuel cells [30].

1.4 State-of-the-art of reliability of power electronics in electro-mobile applications

Reliability is an important issue in the field of power electronics since most of the electrical energy today is processed by power electronics. In most of the electro-mobile applications, e.g. electric and hybrid electric vehicles, power electronic are commonly used in a very harsh environment [1]. Temperature variations, vibration and also humidity stresses are affecting the device (which can come even from the device itself or from external sources) and they may cause unreliable system. Thus, designing reliable power electronic components is important for the aim of reducing the energy losses, maintenance cost and extending the service lifetime as well.

Research within power electronics is of high interest as it has significant impact in the industry of the electro-mobile applications. The reliability of power electronics is affecting the overall system performance in these application fields. The semiconductor devices are some of the most vulnerable components in the power electronic apparatus [31]. Therefore, any fault that occurs in the components will lead to a disorder in the system. These undesired disorders not only affect the safety, but also increases the system operation cost and maintenance [32].

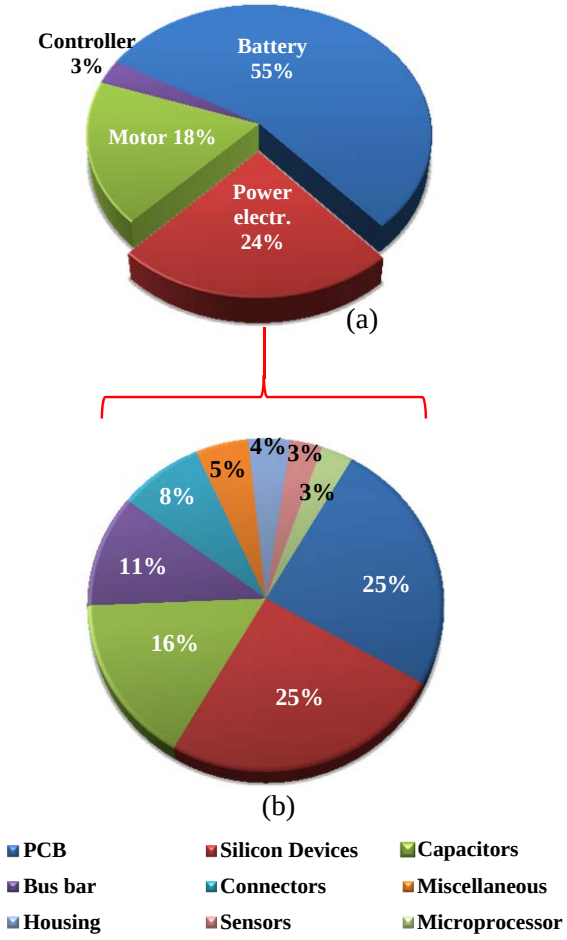


Fig. 1.3: Cost breakdown of power electronics in the hybrid drive system [33]

One of the challenges in the electro-mobility industry is how to improve the reliability of the vehicle's power electronic systems [35]. Sources of failure as vibration, humidity, temperature variations and thermal cycles have an influence on the reliability of power electronics [36]. Fig. 1.3(a) shows the cost breakdown of the hybrid drive system which indicates that 24% of the cost is for power electronics and in Fig. 1.3(b) 50% of the total costs break down of power electronics components is due to the silicon devices and PCB [33], [37].

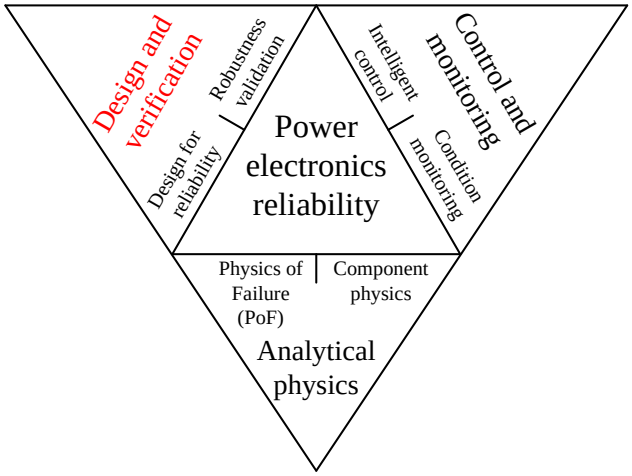


Fig. 1.4: Aspects of power electronics reliability assessment [34].

Furthermore, in today's perspective toward the reliability assessment of power electronic components and systems [34], three main aspects should be considered as shown in Fig. 1.4. Since the typical design target of lifetime in the area of automotive electronics is 15 years [38] and therefore the design and verification are important aspects to the reliability assessment in power electronics which involve different phases as follows:

- Firstly, in this phase analysis is the first step in order to have a full image of the circuit and system. Investigating aspects like stress and strength, failure mode, critical component list and critical component failure mechanism are important.
- The second step is to have an initial design after the analysis, then this design can be optimized considering for example, reliability, power efficiency, power density, robustness and life cycle cost.
- The last step is to verify the design by building prototype, perform calibrated accelerated lifetime tests, reliability and durability analysis before a system finally is in production.

1.5 Sources of failure in power electronics in electro mobile applications

Mapping the sources of failure it could be a method to prevent the creation of failure in the initial design. The classifications of different sources of fail-

ure is shown in Fig. 1.5 for which some of the power electronic components are exposed to and affect their reliability performance. The different sources are discussed in [1] in details. The sources of failure, which have been identified are vibration [39], humidity, thermal cycles [40], [41], and [20], power cycles [42], voltage and current stresses.

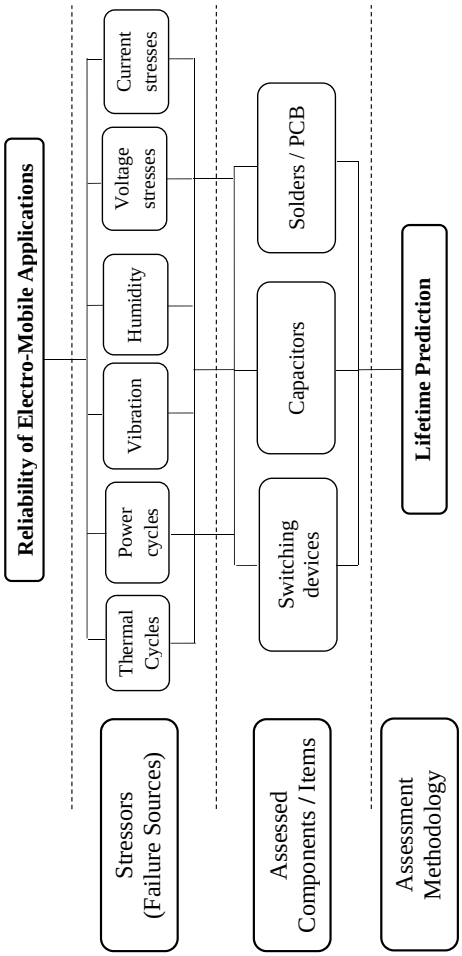


Fig. 1.5: Classification of reliability assessment in electro-mobile applications [1]

1.6 Component failures in power electronics in electro mobility applications

Analysis is the first step to determine which metrics should be investigated in order to evaluate and improve the reliability. Based on a review of condition monitoring for device reliability in power electronic systems presented in [43], semiconductors and soldering failures in device modules are sharing totals 34% of converter system failures as shown in Fig. 1.6.

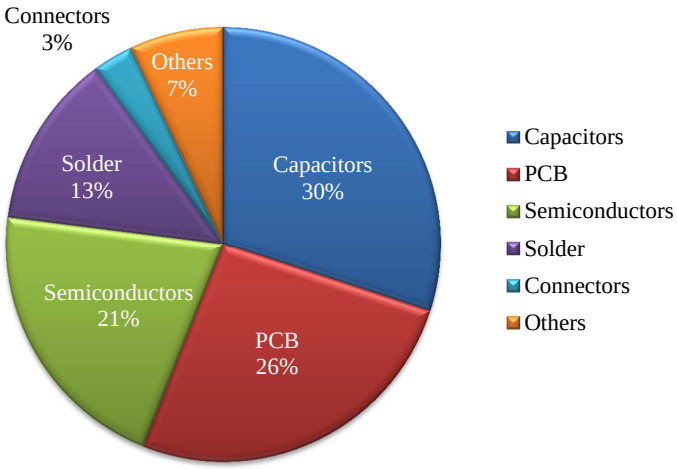


Fig. 1.6: Ranking and failure distribution of power electronic components and sources in power converters [43].

One of the most important challenges in the vehicles manufacture is to consider the component failure rate estimation [44]. Therefore, Fig.1.7 shows an overview during the past 15 years on the components failure and their reliability assessments methods which had been proposed by different researchers in the literature [1]. The switching devices [26] are one of the most critical components that the researchers focused on in the electro-mobile applications. As shown in Fig.1.7, where the red squares refer to the failed components, and the green squares refer to different stressors. It is concluded that the IGBT and chip resistors are critical components according to these specific different research activity in the literature [45], [46], [47], [48], [49], [20], [50], [42], [51], [40], [52], [53], [26], [54], [55], [56], [57], [39], [58], [59], [60], [61], [62], [63] and [64]. It can be concluded from this figure that the thermal cycles are a very common source of failure in the power electronics of the electro-mobile applications.

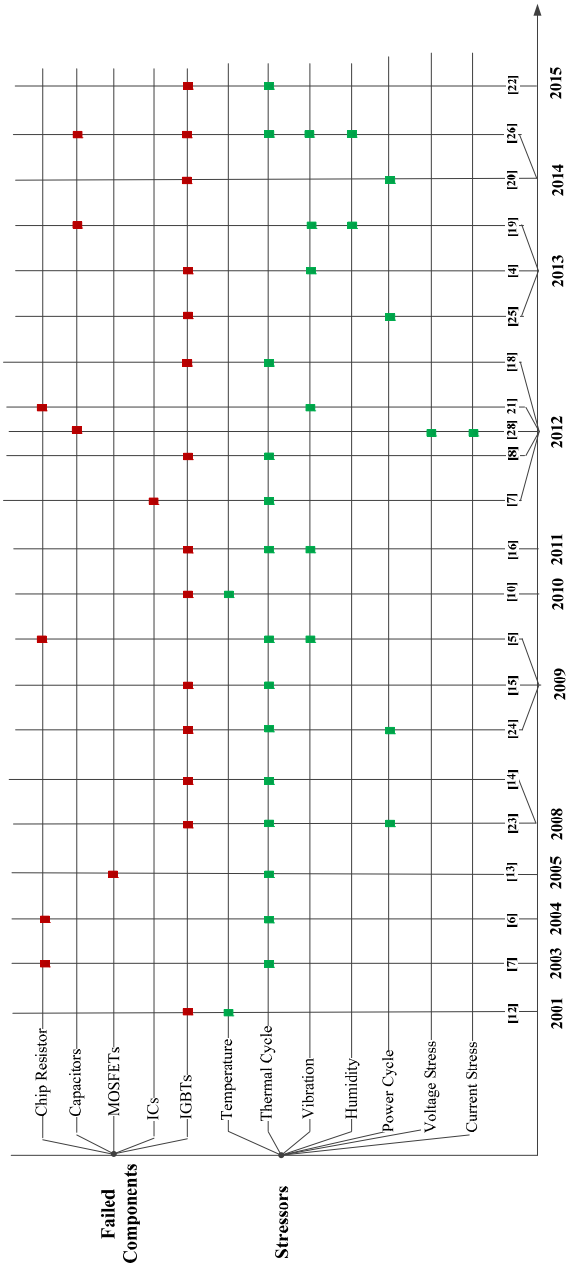
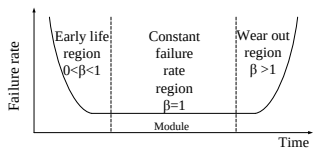
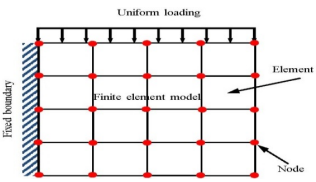
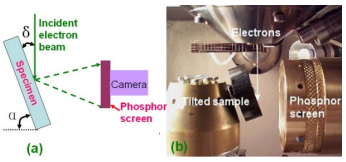
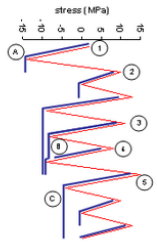


Fig. 1.7: Overview of selected publications which studied sources of failure and failure components of power electronics [1]

1.7 Different lifetime prediction methods

The reliability calculation method is one of the most critical issues, where emerging technologies are studied and the reliability needs to be very high in order to be useful for these types of applications. Table 1.1 shows a summary of some of the established approaches used in the lifetime prediction of some of the power electronic components.

TABLE 1.1 Different methods of lifetime prediction and assessment [1]

Methods	Definitions	Math. Equations	Models
Weibull distribution & Failure rate	Frequently used to model fatigue failure.	$F(t) = 1 - \exp[-(\frac{t}{\eta})^{\beta}]$ F: Probability of failure t: Test statistics (e.g. no. of cycle) η: Characteristics life β: Shape parameter	
Finite element	A numerical method for solving a system of governing equations over a domain of a continuous physical system in to simple geometric shape.	$\{U\} = [K]^{-1}\{F\}$ U: Behavior (e.g. temperature, velocity, …) K: Property (e.g. conductivity, viscosity, …) F: Action (e.g. heat source, force, …)	
Electron backscatter diffraction	A beam of electrons is directed at a point of interest on a tilted crystalline sample by 70°.	$n\lambda = 2d\sin\theta$ n: positive integer λ: is the wavelength of incident wave d: a lattice spacing θ: diffraction angle	
Rain flow counting	A method for counting fatigue cycles from a time history and these fatigue cycles are stress-reversals.	The stress history should be reduced to peaks and valleys by software. (e.g. using Matlab)	

Thus, this field of reliability must be approached at the most fundamental level when evaluating and predicting the products lifetime. Some of the selected lifetime prediction methods are classified in details and Table 1.2 provides an overview on how to be applied for various power electronics

TABLE 1.2 A summary of lifetime prediction based approaches [1].

Assessed Component	Stressor	Based Approach	Ref
Chip Resistors (solders)	Thermal cycling	Weibull model	[7][6][1]
	Thermal cycling Vibration	Electron Backscatter Diffraction (EBSD)	[5]
IGBT	Thermal cycling Vibration	Electron Backscatter Diffraction (EBSD)	[16]
	Temperature	Finite Element Method (FEM)	[12][10]
	Thermal cycling	Finite Element Method (FEM)	[14][15][20] [22]
	Thermal cycling	Weibull model	[8]
	Vibration	Finite Element Method (FEM)	[4]
	Power cycling	Finite Element Method (FEM)	[23][24]
	Thermal cycling	Rain flow counting algorithm	[25]
Capacitors	Thermal cycling	Failure rate model	[19]
	Voltage stresses	Empirical model	[26]
	Current ripple stresses	Life time model	[28]

components.

1.8 Project objectives

The main objective of this project is to investigate the reliability of the Z-source and Y-source power converter from a thermal point of view used in the FCHEV application. This target can be achieved by answering to the following questions:

1) How are the losses inside the converters distributed and their impact on the lifetime of these converters?

2) What are the most critical components, and source of failure in the converter?

3) Does the recently proposed impedance based boost power converter (Z-source and Y-source) offer higher lifetime from a thermal point of view compared to the conventional boost converter?

Thermal investigation is an important aspect to estimate the condition of power electronic components, converters and systems. It is widely applied in reliable or safety critical applications, such as electric vehicles, wind turbines, and photovoltaic, etc.

Due to the aforementioned preamble on reliability and power converters, the thermal investigation is one of the most critical aspects to be considered in modern power converter design.

1.9 Project limitations

The research in this thesis is limited to a collective investigation of the three different topologies (conventional boost, Z-source and Y-source) converters which has not been initiated yet especially with reference to their thermal aspects, loss distribution and also the reliability issues. It is important to study them in order to be designed for long-term reliable usage.

A comparison should be made between the three mentioned topologies in order to select the most appropriate. Common specifications and design parameters are given at different power levels and voltage gains. Loss mapping is presented and compared in the three topologies. Simulation case studies are limited to 20 kW power loading and switching frequency of 20 kHz. The validation of the Y-source converter is limited to 300 W due to the availability of the components in the laboratory. An estimation of the junction temperature is also presented and as well as efficiency measurements when taking all the relevant losses into consideration. Finally, two different lifetime models are performed for the three converters with the applied fuel cell hybrid electric vehicle (FCHEV) application in order to be able to estimate the lifetime of each converter based on the most critical component in the converter.

1.10 Thesis outline

The introduction of this thesis is presented in *Chapter 1*, and includes the background of the project, system configuration of the application, general reliability assessment methods, problem formulation, objectives and limitations.

In *Chapter 2*, the basic operation of the DC/DC boost converters, their theory of operation, specifications and common design parameters for the compared topologies (boost, Z-source and Y-source) converters are given.

In *Chapter 3*, loss modelling and thermal design of the boost DC/DC converters are done. Modelling both the electrical and magnetic losses followed by the thermal design and the estimation of the junction temperature are described.

In *Chapter 4*, the Y-source converter is verified in terms of operation and followed by the a comparison between the three topologies for the same op-

erating conditions (different power loading and voltage gains). In the end the of this chapter a summary is given and the results are discussed.

Chapter 5 presents the reliability assessment method for the applied application. Reliability analysis, lifetime estimation and the mission profile effect on lifetime is discussed and compared between the three topologies.

Finally, conclusions are given including the main contributions, and also the future work in *Chapter 6*.

1.11 List of publications

A list of the papers derived from this project, which are published until now or to be submitted, is given as follows:

Journal Papers

J1. B. Gadalla, E. Schaltz, Y. Siwakoti, F. Blaabjerg,"Investigation of Efficiency and Thermal Performance of the Y-source Converters for a Wide Voltage Range," *Journal of Renewable Energy and Sustainable Development (RESD)*, vol. 1, pp. 300-305, 2015. [Open Access]. ISSN:2356-8569.

J2. B. Gadalla, E. Schaltz, Y. Siwakoti, F. Blaabjerg, "Analysis of loss distribution of Conventional Boost, Z-source and Y-source Converters for wide power and voltage range," *Transaction on Environment and Electrical Engineering*, vol. 2, No. 1, pp. 1-9, 2017. [Open Access].

Conference Contributions

C1. B. Gadalla, E. Schaltz, F. Blaabjerg "A survey on the reliability of power electronics in electro-mobility applications," in *Proc. of IEEE INTERNATIONAL ACEMP - OPTIM - ELECTROMOTION JOINT CONFERENCE: ACEMP – OPTIM*, pp. 304-310, May. 2015.

C2. B. Gadalla, E. Schaltz, Y. Siwakoti, F. Blaabjerg, "Thermal Performance and Efficiency Investigation of Conventional Boost, Z-source and Y-source converters ," in *Proc. of 16 IEEE International Conference on Environment and Electrical Engineering (EEEIC16)*, pp. 1297- 1302, Jun. 2016.

C3. B. Gadalla, E. Schaltz, Y. Siwakoti, F. Blaabjerg, "Loss Distribution and Thermal Behaviour of the Y-source Converter for a Wide Power and Voltage Range," in *Proc. of IEEE 8th International Future Energy Electronics Conference (IFEEC-ECCE Asia)*, pp. 1-6, Jun. 2017.

C4. B. Gadalla, E. Schaltz, D. Zhou, F. Blaabjerg, "Lifetime Prediction of Boost, Z-source and Y-source Converters in Fuel Cell Hybrid Electric Vehicle Application, **[manuscript to be submitted]**.

Chapter. 2

Conventional and Impedance Source DC/DC Boost Converters

In this chapter, basic theories of operation and design of each converter are presented. It is a partially direct copy from my paper [5], and [65], which are published during my PhD study with the following details:

[5] B. Gadalla, E. Schaltz, Y. Siwakoti and F. Blaabjerg, "Analysis of loss distribution of conventional boost, z-source and y-source converters for wide power and voltage range," Trans. on Enviroment and Eectrical Enigneering, vol. 2, no. 1, pp. 1–9, Jan. 2017.

[65] B. Gadalla, E. Schaltz, Y. Siwakoti and F. Blaabjerg, "Loss distribution and thermal behaviour of the y-source converter for a wide power and voltage range," in Proceedings of 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia), pp. 1–6, June 2017.

2.1 Introduction

In conventional boost converters, the needed voltage gain normally requires higher duty cycle, which leads to high conduction losses, voltage and current stresses on the switching devices. However, the abovementioned stressor factors may critically affect the reliability and the lifetime of the power electronic

components as they are thermally loaded high [5], [65].

Recently, impedance source converters have been applied in industrial applications, and hence it has become an interesting topic of research. Researchers have claimed that the proposed impedance source converters have their uniquely advantages such as having a high voltage gain in a small range of duty cycle ratio [66].

Therefore, a comparison between the conventional boost, the Z-source, and the Y-source converters based on the basic design, operational principle, mathematical derivations and parameters selection is presented. Advantages and limitations for each topology is given. Common design and specifications parameters is also discussed in order to have a fair comparison between the three topologies.

This chapter intent to give a detailed study of the compared topologies (boost, Z-source and Y-source) converters. Subsection 2.1 gives the common specification parameters for the three topologies. Section 2.2, 2.3 and 2.4 describes the basic design procedure of the converters, theories of operation. Section 2.5 gives the parameters selection for the boost, Z-source and Y-source respectively. Finally a summary of the studied topologies is given in section 2.6.

2.1.1 Common specification parameters for the compared (Boost, Z-source and Y-source) topologies

In order to have a fair comparison between different topologies many considerations should be taken into account. Especially the efficiency and thermal investigation, which can be done in many different ways. This project is not only investigating the efficiency but also loss mapping models are considered in order to have a better understanding of the nature of each converter.

2.1.1.1 Common Design Parameters

In this part, the common specifications and design parameters are given for the compared topologies (Boost, Z-source and Y-source) converters. These parameters can be summarized as following:

1) The load power P_o = 20 kW, and the output voltage V_{out} = 400 V for both boost factors (2, and 4).

2) The input voltage V_{in} = 100 V for boost factor = 4 and V_{in} = 200 V for boost factor = 2.

3) The switching frequency f_s = 20 kHz.

4) The peak-to-peak ripple inductor current ΔI_{Lp-p} is 20 % of the average inductor current I_L in order to limit the size of the inductance. The higher DC resistance, the higher inductor losses.

5) The peak-to-peak ripple voltage ΔV_{out} is 2 % of the average output voltage V_{out} in order to eliminate the voltage fluctuations across the output voltage.

6) A resistive load applied is R_L = 8 Ω.

In the next sections 2.2, 2.3, and 2.4 the theory of operation of the converters and design formulas are presented.

2.2 Boost converter

A boost converter is a step up converter converting the voltage from low input voltage to higher output voltage requiring a duty cycle (0 <D<1). Its simple theory of operation as well as component count wise allows it to be a competitor with other boosting converters.

2.2.1 Basic theory of operation

The basic structure of the boost converter circuit, the equivalent circuit for the on state mode of operation and the off state mode of operation are shown in Fig 2.1. It compromises of one active switch SW, a diode D_1, an inductor L_1, and a capacitor C_1 for introducing a high voltage boost with (D>0.5). The two modes of operation are as following:

a) During the on state: the switch is closed, the current flows through the inductor and store the energy by the generated magnetic field in the inductor.

b) During the off state: the switch is opened, the current passed will be reduced as the voltage across the inductor is reversed and the magnetic field previously created will decrease to maintain the current flow to the load and the current through the diode will charge the capacitor giving a higher voltage.

The input/output voltage relationship and the duty cycle [67] is expressed in (2.1) as:

$$V_{out} = \frac{V_{in}}{1 - D}, \tag{2.1}$$

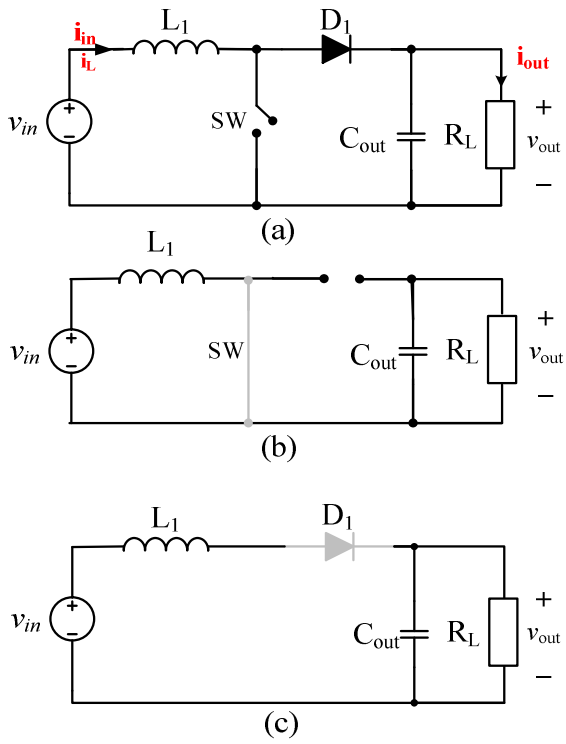


Fig. 2.1: Analysis of the boost converter a) Boost converter circuit topology. b) Equivalent circuit for on state. c) Equivalent circuit for off state.

where V_{out} is the output voltage, V_{in} is the input voltage and D is the duty cycle needed for the required voltage gain.

2.3 Z-source converter

The Z-source converter (ZSC) is an appropriate topology in many alternative energy sources and other different applications [7, 10]. The ZSC has the capability of ideally giving an output voltage up to infinity which of course is not possible due to the limitations of the devices.

2.3.1 Basic theory of operation

The Z-Source converter circuit, and its two modes of operation are shown Fig. 2.2. It consists of two inductors (L_1, L_2) and two capacitors (C_1, C_2) connected in X shape to be coupled to the dc voltage source. The ZSC can produce a

required dc output voltage regardless of the input dc source voltage.

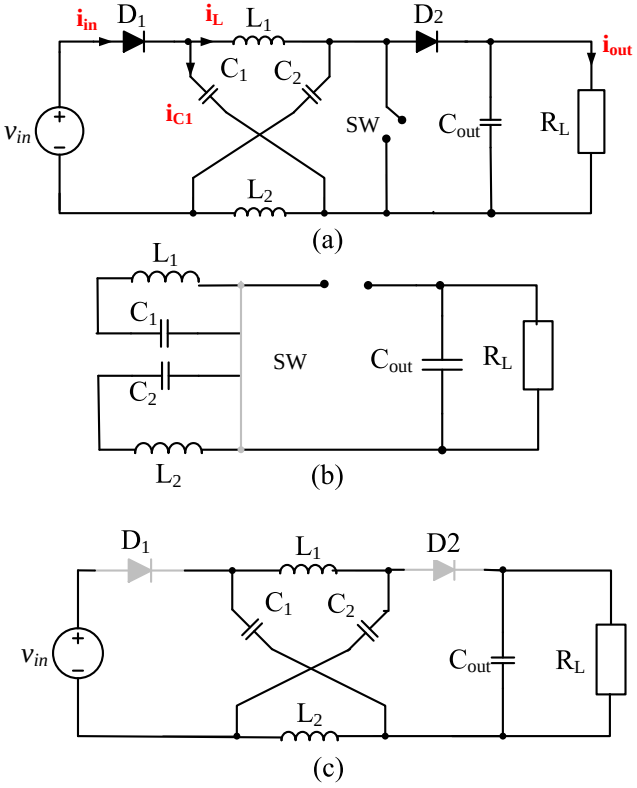


Fig. 2.2: Analysis of the Z-source converter a) Z-Source converter circuit topology. b) Equivalent circuit for on state. c) Equivalent circuit for off state.

The two modes of operation are as the following:

a) In the on state: the switch is closed and the impedance source capacitors (C_1, C_2) release energy to the inductors (L_1, L_2) and then the voltage source and the load will disconnect the Z- source network due to the turn off of the diodes (D_1, D_2). The major concern is the large conduction current passing through the switch during the on state, which may decrease the converter efficiency.

b) In the off state: the switch is opened and the input voltage will supply energy to the load through the two inductors as well as add energy to the two capacitors to compensate the energy lost during the on state.

The input/output voltage relationship and the duty cycle [68] are expressed in (2.2) as:

$$V_{out} = \frac{V_{in}}{1-2D}, \tag{2.2}$$

where V_{out} is the output voltage, V_{in} is the input voltage and D is the duty cycle needed for the required voltage gain.

2.4 Y-source converter

The Y-source converter is a promising topology for higher voltage gain using a small duty ratio and has a very wide range to adjust the voltage gain [4, 13]. The range of duty cycle in the Y-source is narrower than the Z-source and the boost converter but can also boost the voltage.

2.4.1 Basic theory of operation

Fig. 2.3 shows the Y-source impedance network converter and its two modes of operation. It is realized by a three-winding coupled inductor (N_1, N_2, and N_3) for introducing the high boost at a small duty ratio for the SW. It has an active switch SW, two diodes (D_1, D_2), a capacitor C_1, and the windings of the coupled inductor are connected directly to SW and D_1, in order to ensure a very small leakage inductance at its winding terminals.

The two modes of operation are as follows:

a) In the on state: the switch is closed, D_1 and D_2 are off causing the capacitor C_1 to charge the magnetizing inductor of the coupled transformer and the capacitor C_2 to discharge the power to the load.

b) In the off state: the switch is opened, D_1 starts to conduct causing the input voltage to recharge the capacitor C_1 and the energy from the supply and the transformer will also flow to the load. When D_2 starts conducting, it recharges C_2 and the load is to be continuously powered.

The input/output voltage relationship and the duty cycle [13] are expressed in (2.3) as:

$$V_{out} = \frac{V_{in}}{1-KD}, \tag{2.3}$$

where V_{out} is the output voltage, V_{in} is the input voltage, D is the duty cycle and K is the winding factor of the inductance. The winding factor K [13] is calculated according to the turns ratio of the three-winding coupled inductor and it is expressed in (2.4) as:

$$K = \frac{N_1 + N_3}{N_3 - N_2}, \tag{2.4}$$

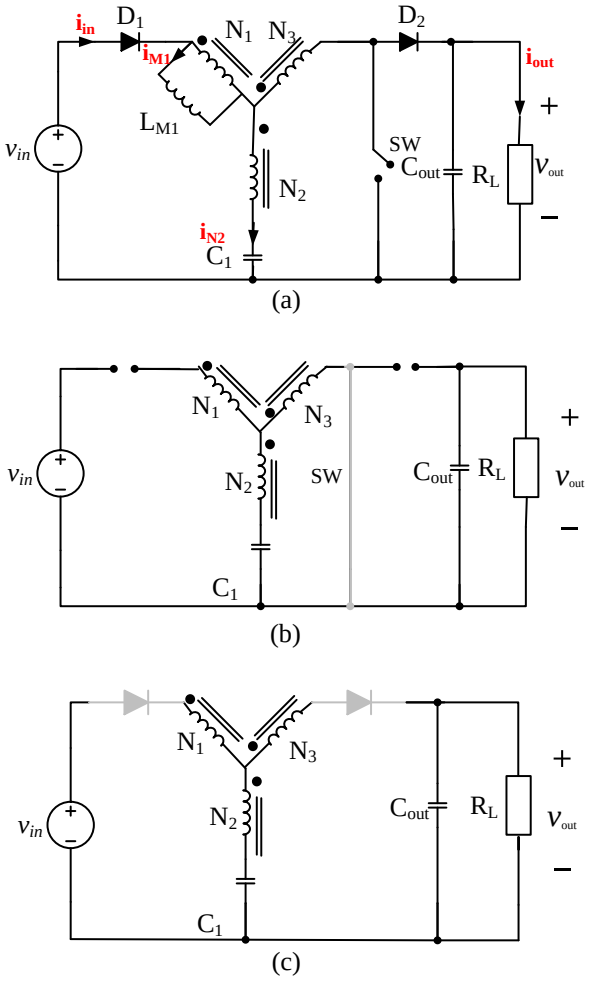


Fig. 2.3: Analysis of the Y-source converter a) Y-source converter circuit topology. b) Equivalent circuit for the on state. c) Equivalent circuit for the off state.

where $(N_1 : N_2 : N_3)$ are the winding ratios of the coupled inductor. A comparison between the inductors, the capacitors design, voltage and current ripples for the three converters is shown in Table 2.1.

2.5 Parameter selection for the boost, Z-source and Y-source converters

Table 2.1 summarizes a comparison between the inductors, the capacitors design, voltage and current ripples for the three converters. As it can be seen in Table 2.1, the current ripple across the inductor ΔI_L is equal to 20% of the inductor current I_L, in the Y-source converter is equal to 20% of the magnetizing current I_M. The voltage ripple across the output capacitor ΔV_{Cout} in the three converter is designed to be 2% of the output voltage V_{out}. The inductor and capacitor values are also listed in Table 2.1 which the duty cycle D, the switching frequency f_s and the resistive load R_L are important factors when designing the suitable values of the desired inductor and capacitor.

2.6 Summary

In this chapter a comparison between the Y-source, Z-source and the conventional boost converter has been performed with respect to their basic design, theory of operation and parameters selection. Common design and specification parameters are also presented in order to have a fair comparison between the three topologies. Considering the load power P_o is 20 kW, the output voltage V_{out} is 400 V for the voltage gains (2 and 4), the switching frequency f_s is 20 kHz, the peak-to-peak ripple current ΔI_{Lp-p} is 2% of the average inductor current I_L, and the peak-to-peak ripple voltage ΔV_{out} is 2 % of the average output voltage V_{out}.

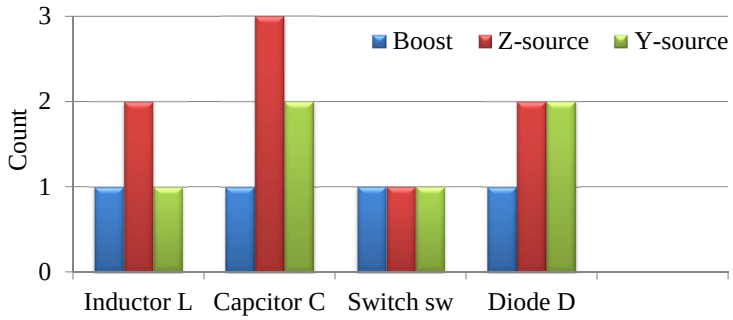


Fig. 2.4: Components count for the Boost, Z-source and Y-source converters

Fig.2.4 summarize the components count for the 3 topologies. It can be seen that the Y-source converter is more intricacy than the Z-source and the conventional boost converters. It can be also concluded that the Z-source and Y-source converters are more expensive than the conventional Boost converter according to the size, and the components count of each topology.

TABLE 2.1 Components design for the Boost, Z-source and Y-source converters [5].

Components	Boost	Z-source	Y-source
Current ripple across inductor	$\Delta I_l = 0.2 \times \frac{P_{out}}{V_{in}} = 20\% I_L$	$\Delta I_l = 20\% I_L$	$\Delta I_l = 20\% I_M$
Voltage ripple across capacitor	$\Delta V_{C_{out}} = 2\% V_{out}$	$\Delta V_C = 2\% V_{out}$	$\Delta V_{C_{out}} = 2\% V_{out}$
Inductor equation	$L = \frac{V_{in} \times D}{\Delta I_L \times f_s}$	$L = L_1 = L_2 = \frac{T_o \times V_c}{\Delta I_L}$ Where, $T_o = DT$	$L^* = A_L N^2 10^{-3}, \quad L_{lik} = \frac{0.292 \times N^{1.056} \times A_c}{L_c}$ $L = L^* + L_{lik}$
Capacitor equation	– $C_{out} = \frac{I_{out(max)} \times D}{f_s \times \Delta V_{out}}$	$C = C_1 = C_2 = \frac{T_o \times I_L}{V_c \times \%\Delta V_c}$ $C_{out} = \frac{V_{out} \times D}{R_l \times f_s \times \Delta V_{out}}$	$C_1 \geq \frac{d_{ST}}{2\%(1-D) f_s} \left(\frac{1}{1-k D} - 1 \right) \frac{P_o}{V_o^2}$ $C_{out} = \frac{V_{out} \times D}{R_l \times f_s \times \Delta V_{out}}$

I_M: Magnetizing current, L_N: Nominal inductance, L_{lik}: Leakage inductance, $T_o = DT = D/f_{sw}$

Chapter. 3

Loss Modelling and Thermal Design of Boost DC/DC converters

3.1 Introduction

Thermal design is a crucial step for power electronic manufactures and also a decisive factor for the reliability assessments [69]. It is involved in all applications but it is particularly important for power semiconductors for two reasons:

1) Semiconductors are very small in size, and they also have low heat capacity and therefore the temperature will rise quickly and need to be contacted properly [70].

2) High current densities operation give a steep temperature rise between junction and ambient.

Reliable thermal design of the power semiconductor is the key to their cost effective utilization due to their limitations. Moreover, in order to have an optimum thermal design the designer should select a proper heat sink or other cooling method [71]. Generally, the main target of the thermal design is the selection of the proper heat sink that should have the following characteristics [72]:

1) The ability to dissipate the semiconductor losses into the surroundings.

2) Keep the junction temperature within safe operating limits.

In the following sections, some of the needed procedures as modelling of all relevant losses are presented in order to have a better thermal design. These procedures can be listed as:

1) Power dissipation in the active device, which are switching losses and conduction losses, where they are in direct related to the duty cycle.

2) Passive elements losses, which are the Equivalent Series Resistance (ESR) losses in the capacitors and the magnetic inductor losses.

3) Estimation of the junction temperature based on models.

This chapter describes the loss modelling and thermal design of the DC/DC boost converters. Section 3.2 describes the electrical loss modelling which are the semiconductors losses (switching and conduction losses). The heat sink specifications and passive elements loss modelling are also discussed. Section 3.3 discuss the temperature modelling. Section 3.4 gives a summary of the studied investigation.

3.2 Modelling of the electrical losses

3.2.1 Semiconductors losses

1) Switching losses occur when the device is transitioning from the blocking state to the conducting state and vice-versa [73]. This interval is characterized by a significant voltage across its terminals and a significant current through it. The energy dissipated in each transition needs to be multiplied by the switching frequency to in order to obtain the switching losses. The switching losses P_{sw} are expressed in (3.1) as:

$$P_{sw} = \left(E_{on} + E_{off}\right) \times f_{sw}, \tag{3.1}$$

where E_{on} and E_{off} are the energy losses during turn on and turn off of the switch, f_{sw} is the switching frequency.

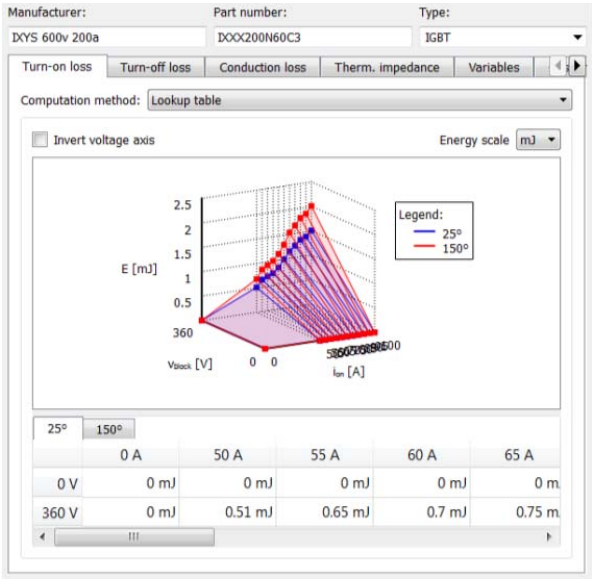
2) Conduction losses appear when the device is in full conduction mode [73]. The average conduction losses P_{cond} are expressed in (3.2) as:

$$P_{cond} = R_{(on)} \times I^2_{sw(RMS)}, \tag{3.2}$$

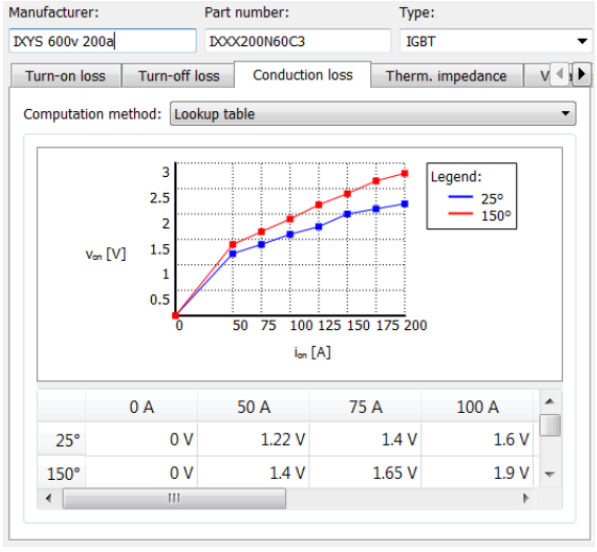
where $R_{(on)}$ is the resistance of the selected switch, $I_{sw(RMS)}$ is the root mean square current passing through the switch. The switching time period T is as given in (3.3):

$$T = \frac{1}{f_{sw}} \tag{3.3}$$

where f_{sw} is inversely proportional to the time period T.



(a)



(b)

Fig. 3.1: (a) Mapping of the *switching* losses in PLECS toolbox. (b) Mapping of the *conduction* losses in PLECS toolbox.

In Fig. 3.1 the switching and conduction losses are calculated according to the thermal models inserted into the thermal library of the PLECS tool-

box. Using the data sheet information of an IGBT rated at 600 V and 200 A as an example. Mapping between the turn on and off energies for the device (IGBT), at different temperature levels (25°C and 150°C), at only (360 V) blocking voltage according to the available data from the manufacture in the data sheet the current range is from (0 to 200 A), which describe the calculations of the switching and conduction losses in the simulation model.

3.2.2 Capacitor ESR loss

The capacitor Equivalent Series Resistance (*ESR*) is "the value of the resistance, which is equal to the total effect of a large set of energy loss mechanisms occurring under the operating conditions where it can be a parameter to measure the capacitor losses" [74]. The capacitor losses are expressed in (3.17) as:

$$P_{cap.loss} = I_{cap.}^2 \times ESR \tag{3.4}$$

where $I_{cap.}$ is the rms current passing through the capacitor, and ESR is the equivalent series resistance measuring the effect of the losses dissipated in the capacitor.

3.2.3 Inductor loss

3.2.3.1 Magnetic core design

In this part, two different types of cores loss modelling are selected for the voltage gain of 2 (high flux 58337 core) and voltage gain of 4 (Metglas powerlite C-core) using two different methods (selection of the optimum powder core from Magnetics and commonly used K_g method). The magnetic core design [75] is done through the following steps:

1) In order to select a proper core size, the DC current I_{DC} in Ampere and the inductance L in mili Henry required with DC bias should be known to select the core from the core selector chart according to the calculated value (mH.A^2) in (3.5):

$$LI_{DC}^2 = \text{value}. \tag{3.5}$$

A high flux 58337 core [75] was selected for the three converters using the voltage gain of 2.

2) Inductance, core size and permeability are now known, then calculating the no. of turns by determining the minimum inductance factor A_{Lmin} by using the worst case negative tolerance (generally -8%) given in the core data sheet in (3.6) and (3.7)as:

$$A_{lmin} = A_l - 0.08Al, \tag{3.6}$$

$$N = \sqrt{\frac{L \times 10^3}{A_{lmin}}}, \tag{3.7}$$

where A_{lmin} is the minimum inductance factor (nH/T^2), and L is the inductance in (μH).

3) Choosing the suitable wire size according to the rated power and calculated number of turns (N), is the last step before calculating the DC resistance according to the wire size with a window fill factor assumed to be 40% in (3.8) as:

$$C_A = \frac{W_f \times W_A}{N}, \tag{3.8}$$

where C_A is the wire area, W_f in the window fill factor, and N is the no. of turns.

4) The DC resistance can be determined after knowing the winding factor of the core, wire gauge (AWG), and the no. of turns. The DC resistance can be calculated in (3.9) as:

$$R_{DC} = MLT \times N \times \Omega/Length, \tag{3.9}$$

where MLT is the mean length per turn, and $\Omega/Length$ is the resistance per meter. Furthermore, in the voltage gain of 4 METGLAS power-lite C-core [39] is used, since it has extremely low core loss and high permeability which are required with higher voltage gains. The design steps are based on the K_g method [76].

3.2.3.2 Core loss

The calculation of the core loss of magnetic materials is based on Steinmetz's equation, which is a physics based equation. The core losses are expressed in (3.10):

$$P_v = k f^{\alpha} \hat{B}^{\beta}, \tag{3.10}$$

where $\hat{B}$ is the peak flux density excitation with frequency f, P_v is the time-average power loss per unit volume, and (α, β, k) are material parameters found by curve fitting. The improved generalized Steinmetz's equation is expressed in (3.11) as:

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} \left(\Delta B^{\beta-\alpha}\right) dt, \tag{3.11}$$

where ΔB is the flux density from peak to peak and in (3.12):

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |cos\theta|^{\alpha} \times 2^{\beta-\alpha} d\theta}, \tag{3.12}$$

where θ is the angle of the sinusoidal waveform simulated.

3.2.3.3 DC and AC Winding loss

The copper losses in the winding describe the energy dissipated by the resistance in the wire used in the coil. It is divided into two types (DC and AC winding loss).

1) The DC winding losses can be calculated in (3.13) as:

$$P_{DC} = I_{av}^2 \times R_{DC} \tag{3.13}$$

where *(P_{DC})* is the DC copper losses in the winding, I_{av} is the average current passing through the wire, and R_{DC} is the DC resistance of the wire.

2) AC copper losses can be significant for large current ripple and for higher frequency. It can be calculated through the skin effect, where the current density is an exponentially decaying function of the distance into the wire, with the characteristic length δ is known as the skin depth in (3.14) as:

$$\delta = \frac{7.5}{\sqrt{f_s}}, \tag{3.14}$$

where δ is the skin depth in cm, and f_s is the switching frequency which in our design is 20 kHz.

In order to calculate the AC resistance R_{AC}, the thickness h of the wire should be known since it is a function of the DC resistance R_{DC} which can be calculated in (3.15) as:

$$R_{AC} = \frac{h}{\delta} \times R_{DC}, \tag{3.15}$$

where h is the thickness of the wire in cm. The AC winding losses can be calculated as given in (3.16) as:

$$P_{AC} = I_{AC-rms}^2 \times R_{AC} \tag{3.16}$$

where P_{AC} is the AC winding loss, I_{AC-rms} is AC ripple rms current passing through the wire, and R_{AC} is the AC winding resistance.

3.3 Temperature Modelling

3.3.1 Procedures for heat sink design

A heat sink is the cooling device to absorb the thermal losses dissipated by the components within its boundaries using natural, forced convection and/or fluid cooling can be used if needed. The heat sink is designed separately for each boost factor. The thermal equivalent demonstration for the total power losses (switching and conduction loss), the thermal resistance from junction to ambient is shown in Fig. 3.2.

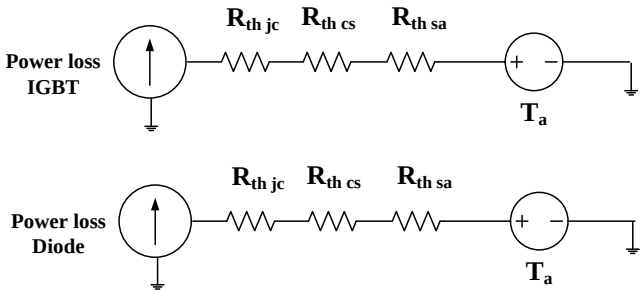


Fig. 3.2: Simplified thermal equivalent circuit of total power losses with their thermal model in PLECS toolbox

The thermal resistance is an important parameters for the semiconductor device. It depends on structural and material properties of the device (interfaces, dimensions and thermal conductivity of materials). It will give an immediate information on the thermal properties of the device and will give the size and the use of a heat sink for a safe operation. The thermal resistance is a parameter used for steady state operation which can provide the temperature level after an initial transient phase, but does not reveal any information about the thermal behaviour in dynamic conditions.

The choice of a proper heat sink depends on the maximum allowable junction temperature that the device can tolerate. Assuming 125°C as a maximum junction temperature for the devices as a specification for the heat sink. The ambient temperature is set to 25 °C in this investigation.

1) In order to know if the natural/forced convection is needed the maximum allowable thermal resistance from junction-to-ambient need to be known in (3.17) as:

$$R_{ja-IGBT} = \frac{T_{j,max} - T_{a,max}}{P_{loss}}, \tag{3.17}$$

where $R_{ja-IGBT}$ is the junction to ambient thermal resistance of the IGBT, $T_{j,max}$ is maximum junction temperature, $T_{a,max}$ is the maximum ambient thermal resistance and P_{loss} is the total power loss dissipated by the IGBT.

2) According to the calculated value of the maximum allowable thermal resistance from junction-to-ambient, a decision can be made whether natural or forced cooling should be selected. Then the total thermal resistance from junction to ambient is calculated in (3.18) as:

$$R_{th-ja} = R_{th-jc} + R_{th-cs} + R_{th-sa}, \tag{3.18}$$

where R_{th-ja} is the thermal resistance from junction to ambient, R_{th-jc} is the thermal resistance from junction to case, R_{th-cs} is the thermal resistance from case to heat sink and R_{th-sa} is the thermal resistance from heat sink to ambient.

3) If the calculated maximum allowable thermal resistance from junction-to-ambient is very small, that means that a large heat sink is needed for natural convection.

The thermal resistance needed for the heat sink is given in (3.19) as:

$$R_{th-sa} = R_{th-ja} - R_{th-jc} + R_{th-cs}, \tag{3.19}$$

where R_{th-jc} is the thermal resistance from junction to case and is given in the data sheet of the device, R_{th-cs} is the thermal resistance from case to heat sink or the thermal grease resistance, which can also be found in the data sheet or calculating its value according to the type of material used for isolation. For example, the thermal grease resistance of Silicon-Free type of interface thickness 0.164 mm, thermal conductivity is 0.79 $W/m^{\circ}C$ and operating temperature range is from -40 to 200 $^{\circ}C$ can be calculated in (3.20) as:

$$R_{th-cs} = \frac{\text{interface thickness}(mm) \times 1000}{\text{thermal conductivity}(W/m^{\circ}C) \times \text{contact area}(mm^2)} \tag{3.20}$$

4) According to the calculated R_{th-sa}, a heat sink can be chosen as e.g. FISHER ELECTRONI part no. LA 9/100 230 V. Fig. 3.3 shows the heat sink chosen thermal resistance 0.28 ($°C/W$) for the devices which are thermally separated and fit with the thermal resistances of the devices calculated in (3.19).

Fig. 3.3: FISHER ELECTRONIK LA 9/100 230 V heat sink [77].

3.3.2 Estimation of the junction temperature at different power loading

Simple thermal equations are frequently used to calculate junction temperature in steady state as in (3.22). PLECS tool box is used to estimate the junction temperature T_j depending on the thermal model of the devices in the data sheet known as the thermal resistance R_{th}.

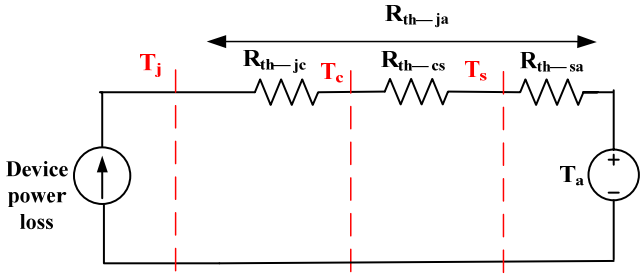


Fig. 3.4: General electro-thermal network of semiconductor devices

As shown in Fig. 3.4, a general representation for the electro thermal network, where R_{th-jc} is the junction to case thermal resistance, R_{th-cs} is the case to heat sink thermal resistance, R_{sa} is the heat sink to ambient thermal

resistance, which are an example of a thermal model, in order to be able to calculate the junction temperature T_j.

Calculating the R_{th-ja} ($^\circ C/W$) of the device and assuming ambient temperature at 25 $^\circ C$ allows to estimate the rise of the junction temperature inside the devices in (3.21) as:

$$\Delta T_{Device} = P_{loss} \times R_{th-ja}, \tag{3.21}$$

where ΔT_{Device} is the rise in the device temperature, P_{loss} is the total power loss generated from the device, and R_{th-ja} is the junction to ambient thermal resistance. The junction temperature of the device T_j is calculated in (3.22) as:

$$T_j = \Delta T_{Device} + T_a, \tag{3.22}$$

where T_a is the ambient temperature.

Fig. 3.5 shows an example of a Foster model build into the PLECS toolbox, where from R_1 to R_4 is the total thermal impedance for the junction to case thermal resistance of the device in Kelvin/Watt and τ is the thermal time constant in second, in order to be able to estimate the junction temperature T_j.

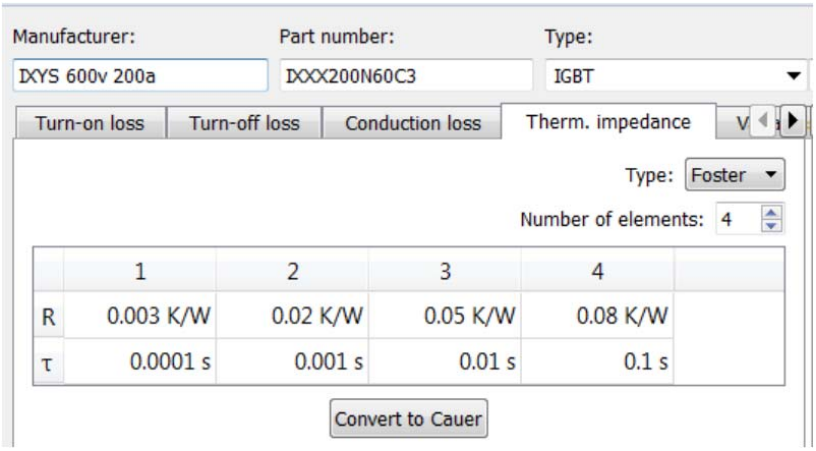


Fig. 3.5: Thermal impedance Foster model for an IGBT in the thermal description block of PLECS toolbox

3.4 Summary

The power loss models and thermal modelling are presented in this chapter. The temperatures calculated in these conditions are all steady state temperatures. Thermal design procedures of the DC/DC boost converters is presented. Electrical loss modelling which models the semiconductors losses (switching and conduction losses) and passive elements loss modelling which are (capacitor ESR and magnetic core losses) are also presented. Heat sink specifications and a proper design of the heat sink is also presented. It is important to a have proper design for the heat sink in order to maintain the device availability in a safe operation mode by decreasing the thermal stress generated from the device. Moreover, how to estimate and get a full image of the devices junction temperature is also given.

Chapter. 4

Investigation of DC/DC Boost Converters

In this chapter, an investiagtion of the DC/DC boost converters and the validation of the Y-source converter are presented. This chapter is one of the main contributions in this PhD project and part of it is a direct copy from two papers [78], and [65] which are published during my PhD study with the following details:

[78] B. Gadalla, E. Schaltz, Y. Siwakoti and F. Blaabjerg, "Thermal performance and efficiency investigation of conventional boost, z-source and y-source converters," in 2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC), June 2016, pp. 1–6.

[65] B. Gadalla, E. Schaltz, Y. Siwakoti and F. Blaabjerg,"Loss distribution and thermal behaviour of the y-source converter for a wide power and voltage range," in Proceedings of 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia), June 2017, pp. 1–6.

4.1 Introduction

In this chapter a comparison has been made between the conventional boost, Z-source and Y-source converters from their efficiency and loss distribution point of view based on the thermal evaluation of the semiconductors. In

order to a have a fair realistic comparison between three different topologies, some design parameters need to be the same as presented in Chapter 2.

The PLECS toolbox is used for the three converter analysis. It should be kept in mind that the losses are calculated as an average value for a load conditions when it reaches steady state value. The parameters selection for each converter are compared according to the passive components counts and their voltage and current ripples are as specified in Table 2.1 in Chapter 2. The same is the case for the switching devices, which are designed according to each converter requirements for the voltage and current ratings.

In this chapter Section 4.2 gives the general simulation models used for the three topologies. Section 4.3 gives the results of the Y-source converter. Section 4.4, 4.5 and 4.6 discuss the simulation results of the three compared topologies at different voltages and power levels. Section 4.7 gives the conclusion and summary of the compared studied topologies.

4.2 Loss Model Implementation in PLECS

In this section, a general description of the used blocks (switching, conduction, capacitor ESR, magnetic losses) in the PLECS toolbox is described. In Fig. 4.1 a demonstration of how to measure the switching and conduction losses in PLECS is done.

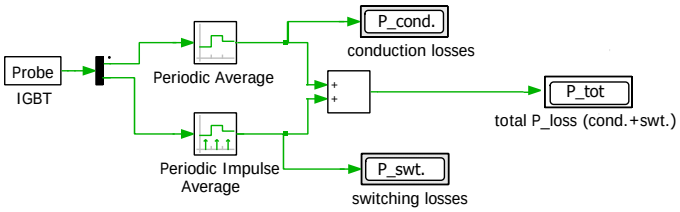


Fig. 4.1: Switching and conduction losses block in PLECS toolbox

1) The semiconductor device (IGBT and Diode) is added inside each probe and includes both switching and conduction losses in order to be able to calculate the losses generated from the semiconductor device.

2) The conduction loss can be measured through the periodic average block, which periodically averages a continuous input signal over a specified averaging time. The output is updated at the end of each average period suited to determine the average conduction losses of the power semiconductors.

3) Switching loss can be measured through the periodic impulse average block, which periodically averages an input signal consisting of a series of Dirac impulses. The output is updated at the end of each average period suited to determine average switching losses of the power semiconductors.

The same idea is valid for the capacitor losses, as the measured current passing through the capacitor is inserted inside the probe function and a constant value of the Equivalent Series Resistance (ESR) is inserted inside a constant block in order to have an instantaneous average value of the capacitor ESR losses. In Fig. 4.2 is the total magnetic loss measured according to the Steinmetz equation as given in equations from (3.10) to (3.13).

1) In probe 4 in Fig. 4.2, the flux meter rate is inserted which is able to measure the rate-of-change of the magnetic flux ϕ through the component and provides it as a signal at the output and then connected to the $'K'$ block which consists of a gain, which is the inverse of the area of the core A_c.

2) In probe 5 in Fig. 4.2, the linear core is dragged into measure the magnetic flux density. Connecting both probes (4 and 5) to block $'X'$ which contains the parameters of the core as (volume (g^3), (α, β, k) are the material parameters found by curve fitting and the excitation period $\frac{1}{f}$) give the calculation of the core losses.

3) In the copper loss block, the probe inside contains the DC resistance (R_{DC}) connected to the periodic average block to measure the DC winding losses.

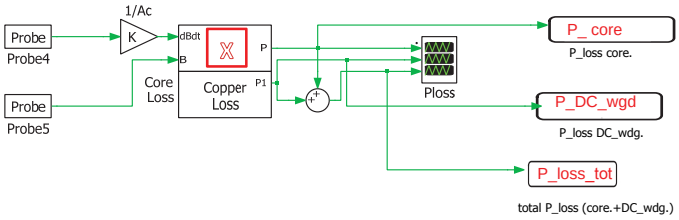


Fig. 4.2: Magnetic (core, and winding) losses block used in PLECS toolbox

In the next sections, the Y-source converter is scaled down from 20 kW to 300 W, due to the limitations in the laboratory and in order to prove the concept of operating principle, as well as see the shapes of the obtained currents and voltages waveforms.

The study of the Y-source converter at 300 W rated power to validate the loss and the temperature modelling discussed in Chapter 3. Further,

presenting the simulation results for the three compared converters at the maximum power rating of 20 kW and different voltage gains. The simulation results of the operated junction temperature T_j and the calculated efficiencies η are also given under different power loadings. Finally, the distribution of the losses of the three converters are summarized in dedicated charts for each voltage gain and at 20 kW rated power separately.

4.3 Validation of the Y-source converter

In this section, the Y-source converter was selected to validate the models developed. Due to complexity of the Y-source, which needs to be understood and it is recently proposed compared to the Z-source and boost converters.

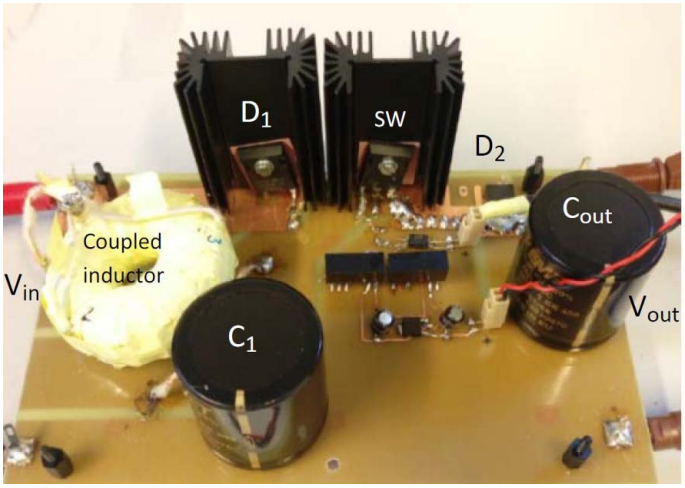


Fig. 4.3: The Y-source converter prototype.

A prototype has been designed for the components, semiconductors ratings, selecting a proper core and heat sink [79] for 300 W rated power. Using Altium designer for drawing the circuit layout and printing the PCB afterwards, all components have been soldered and the prototype has been tested with a resistive load. An experimental prototype of the Y-source converter shown in Fig. 4.3 is used for this investigation.

The main purpose of the validation is to compare the efficiency and the total switch (MOSFET) losses obtained from the simulation model. The same operating conditions are applied as listed in Table 4.1, in order to have a realistic comparison between the simulation model and the prototype. Both the simulated and obtained experimental waveforms are compared and discussed in the following subsections.

TABLE 4.1 Specifications and simulation parameters of the Y-source converter prototype [78].

Parameter	Value / description
Rated power (P)	300 W
Voltage gain	4
Winding factor (K) , $K = \frac{N_1 + N_3}{N_3 - N_2}$	4
Input voltage (V_{in})	60 V
Output voltage (V_{out})	240 V
Duty cycle (d_{st})	0.1875
Turns ratio of coupled inductor (N_1:N_2:N_3)	5:1:3
No. of turns (N_1:N_2:N_3)	80:16:48
Core	MPP C055863A2
Switching frequency (f_s)	20 kHz
Capacitors	C_{in} = 470 µF, 400 V Kemet C_1 = 470 µF, 400 V Kemet C_2 = 470 µF, 400 V Kemet
Heat sink (ABL)	173AB, 0.48 °C/W
Switch (Mosfet)	C2M0040120D, 1200 V, 60 A
Diode D_1	C3D25170H, 1700 V, 26.3 A
Diode D_2	C3D20060D, 600 V, 20 A

4.3.1 Simulation results for the Y-source converter at 300 W loaded power and voltage gain 4

The analysis of the loss distribution and junction temperature measurement in the Y-source converter is performed.

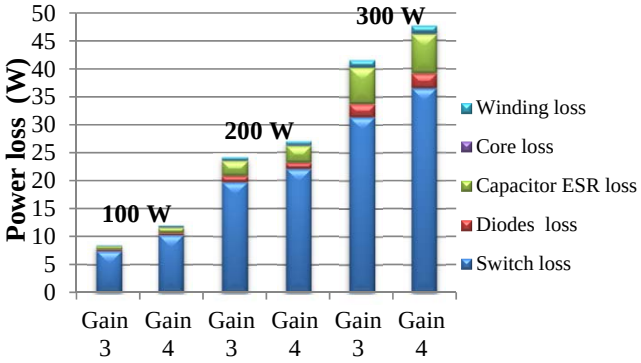


Fig. 4.4: Simulation results of different losses distribution for the Y-source converter at 100 W, 200 W and 300 W loading and different voltage gain (3 and 4).

Fig. 4.4 shows the loss distribution for the simulated converter at three different power levels (100 W, 200 W, and 300 W) and two different voltage gains (3 and 4).

The switch loss indicated in Fig. 4.4 is for the total losses (switching and

conduction loss) generated from the MOSFET, the diodes loss is the total losses for (D_1 and D_2). In the winding loss, only the DC winding loss is presented since the AC winding loss is very small so it is neglected. It can be seen from the losses distribution that the losses of the switch are highest power loss at all different power levels and voltage gains.

It is also seen in Fig. 4.4 that reducing the power level from 300 W to 200 W has a significant influence on the loss reduction of the switch and capacitor losses, whereas further reducing to 100 W reduces the loss approximately to half. Furthermore, there are slightly difference in the estimated power losses between the voltage gain (3 and 4), regardless the power level and with no doubt the power losses in voltage gain 4 is higher than in the voltage gain 3.

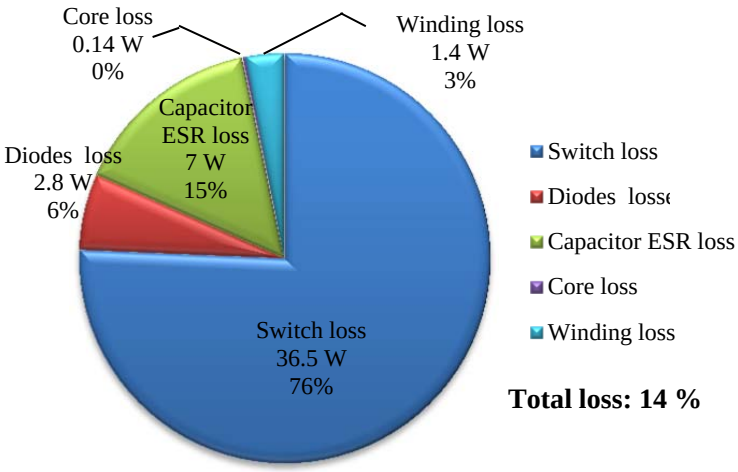


Fig. 4.5: Power losses distribution for the Y-source converter at 300 W power loading and using a voltage gain of 4.

Fig. 4.5 shows detailed analysis for losses distribution of the converter at 300 W rated power and voltage gain of 4. The results indicate that the switch losses is 76%, the total conduction losses of the two diodes (D_1 and D_2) are 6%, the capacitor losses are 15%, and the heat loss generated from the winding loss which are 3% of the total loss.

Furthermore, some of the basic waveforms from using simulations of the Y-source converter at 300 W rated power and voltage gain of 4 is presented in Fig. 4.6 where the input/out side simulated waveforms are shown ((v_{in}), (i_{in}), (v_{out}) and (i_{out})) and compared with the obtained waveforms from the prototype.

As a part of the validation for the Y-source converter, in Fig. 4.7 the voltage (v_{sw}) and current (i_{sw}) of the (switch) MOSFET, and the current

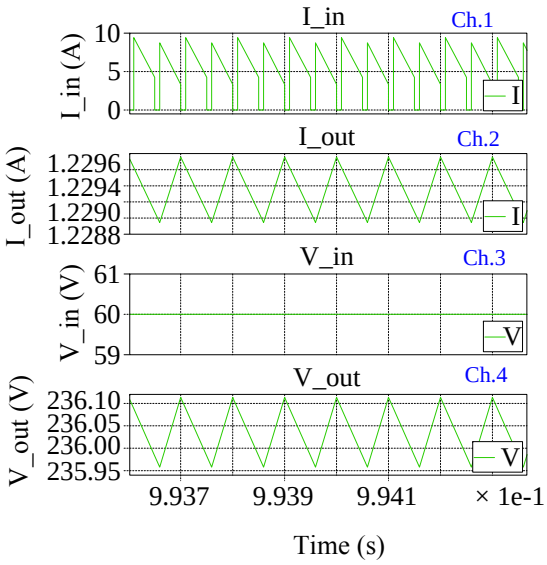


Fig. 4.6: Simulation waveforms of the Y-source converter with k = 4 and d_{st} = 0.19 Where, Ch. 1: input current (i_{in}), Ch. 2: output current (i_{out}), Ch. 3: input voltage (v_{in}). , and Ch.4: output voltage (v_{out}) in voltage gain 4.

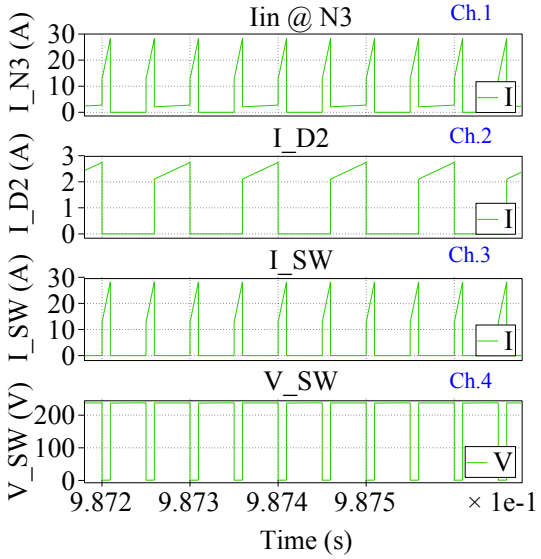


Fig. 4.7: Simulation waveforms of the Y-source converter with k = 4 and d_{st} = 0.19 at its zoom view Where, Ch. 1: current through winding N_3 , Ch. 2: current through diode D_2 (i_{D_2}), Ch. 3: current through SW (i_{sw}), and Ch. 4: Switch voltage (v_{SW}) in voltage gain 4.

(i_{D_2}) through diode D_2, and current (i_{N_3}) passing through the winding N_3 is shown.

4.3.2 Validation results for the Y-source converter at 300 W loaded power and voltage gain 4

In this subsection, the prototype of the Y-source is tested under the same rating conditions as in the simulation model in order to start the validation steps. The input/output voltage sides, the voltage gain, and the general efficiency are measured. Further, all the currents and the voltages through each component in the prototype is measured in order to measure all the losses.

In Fig. 4.8 different experimental current and voltage waveforms in the converter are shown where they are as expected under the same conditions for 300 W rated power and voltage gain 4. The input/output sides are shown $((v_{in})$, (i_{in}), (v_{out}) and $(i_{out}))$, where they are compared and matches the rms simulated waveforms. It is decided to show the switch loss results, since they are the highest generated losses in the converter as shown in the simulation results. Further it is foreseeable from the efficiency measurement of the prototype as shown in Fig. 4.8.

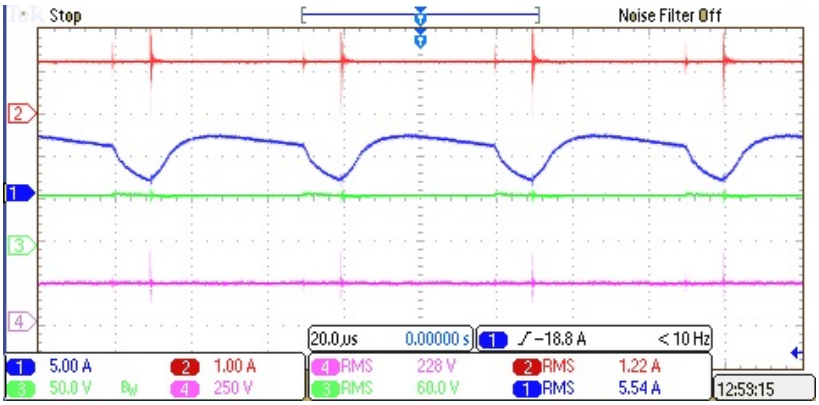


Fig. 4.8: Experimental waveforms of the Y-source converter with k = 4 and d_{st} = 0.19 at its zoom view where, Ch. 1: input current (i_{in}), Ch. 2: output current (i_{out}), Ch. 3: input voltage (v_{in}). , and Ch.4: output voltage (v_{out}).

In order to verify the switch loss modelling, the drain to source voltage (v_{ds}) is measured by a voltage probe and the current passing through the switch (i_{ds}) is measured through the math operation in the oscilloscope. The total power loss of the switch is then calculated and compared with simulated one in order to verify the total switch loss as shown in Fig. 4.9.

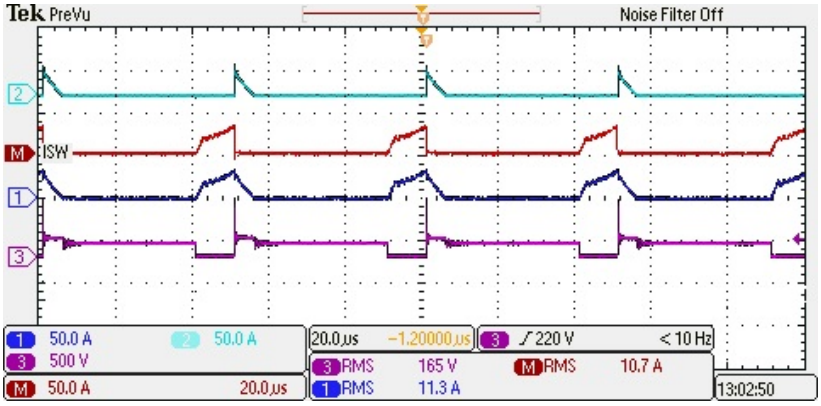


Fig. 4.9: Experimental waveforms of the Y-source converter with k = 4 and d_{st} = 0.19 at its zoom view where, Ch. 1: current through winding N_3 , Ch. 2: current through diode D_2 (i_{D_2}), Ch. M: current through SW (i_{sw}) obtained through the math opertaion on the osciliscope, and Ch.4: drain to source voltage (v_{DS}).

The total efficiency is an important factor in this analysis, since not all the relevant losses can be measured directly from the prototype. The total efficiency of the converter can be measured in both the simulation model and in the prototype from and it is calculated to be Fig. 4.8 where the output/input signals can be easily calculate the efficiency to be $(P_{out})/(P_{in})$= 84%, while in the simulation model it is equal to 86%.

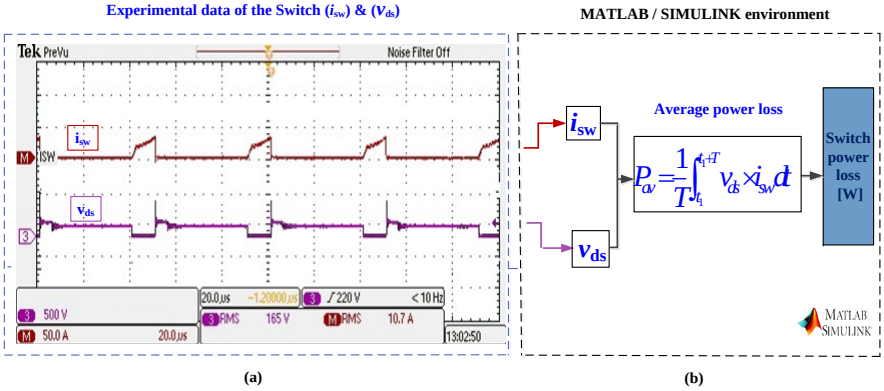


Fig. 4.10: Illustration diagram of the switch loss calculation in the Y-source converter prototype. a) waveform of the switch current (i_{sw}) and switch volatge (v_{ds}). b) calculation method.

As stated earlier, the loss calculations in the Y-source converter simulation model are performed using the PLECS toolbox. Since the power losses of the switch could not be measured directly, the total switch loss is calculated

based on the switch voltage and current measurements.

Therefore, in order to validate the loss calculations in the Y-source prototype converter, the switch voltage (v_{ds}) and current (i_{sw}) waveforms obtained from the prototype are processed in Matlab as shown in Fig. 4.10. In the simulation model the total switch losses is 36.5 W, and the measured average power loss from the processed data through Matlab is 38.5 W.

4.4 Simulation results for the boost converter under different power loadings and voltage gains

In this section the simulation model of the boost converter implemented in the PLECS toolbox is shown in Fig. 4.11. The function blocks shown in this figure are used in the loss mapping analysis as explained earlier in Chapter 3.

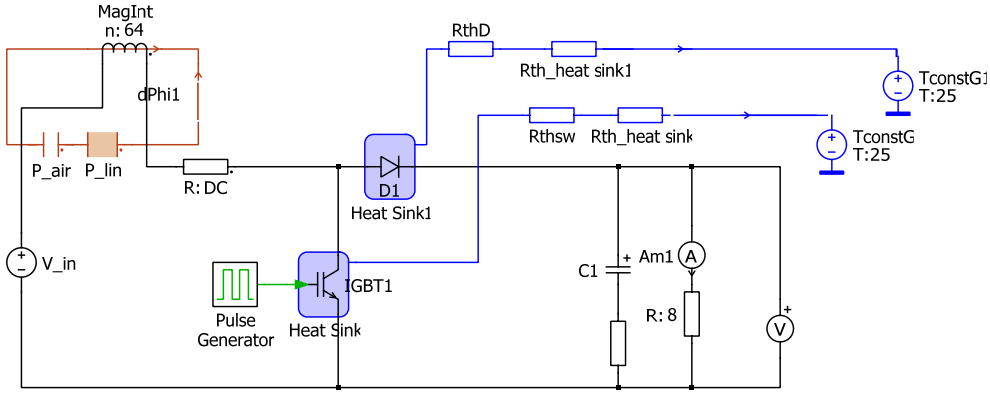


Fig. 4.11: Schematic diagram of boost converter in PLECS.

It consists of a DC source at the input voltage side, a linear magnetic core with a certain number of turns depending on the calculated inductor value. The semiconductors devices (IGBT, and diode) are placed with heat sinks in order to be able to measure the device losses (switching and condition losses) as well as estimating the junction temperature of the devices. An output capacitor and a resistive load is placed at the output side in order to be able to measure the output voltage and the output current through the voltmeter and ampere meter placed at the output side.

In the the following subsection, some of the obtained waveforms from the simulation model of the boost converter are presented under two different voltage gains (2, and 4).

4.4.1 Basic waveforms of boost converter using voltage gain 2 and 4

In this subsection, it can be seen than the switch current is almost doubled from voltage gain 2 to 4 and the switch voltage level are the same. In Fig. 4.12 (a) the generated switch voltage and current at voltage gain two is shown which matches the calculated values of these voltages and currents.

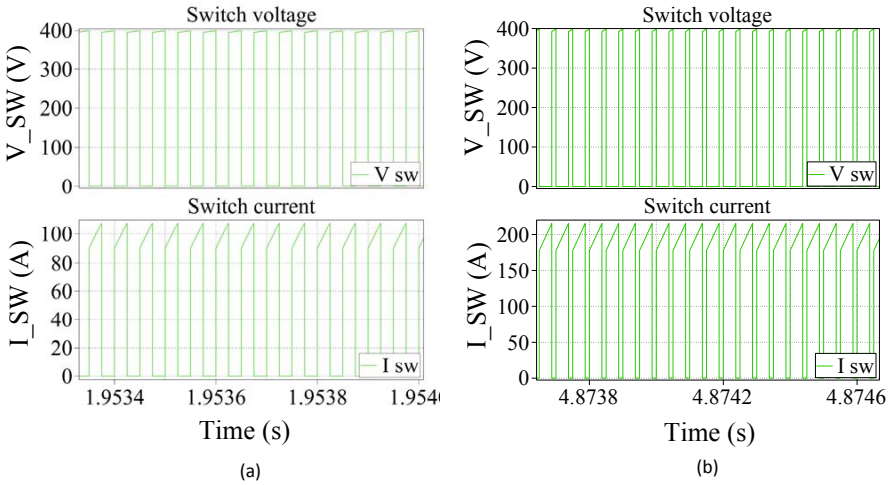


Fig. 4.12: Generated waveforms for the voltage and current across a) Switch using voltage gain 2 b) Switch using voltage gain 4 of the Boost converter.

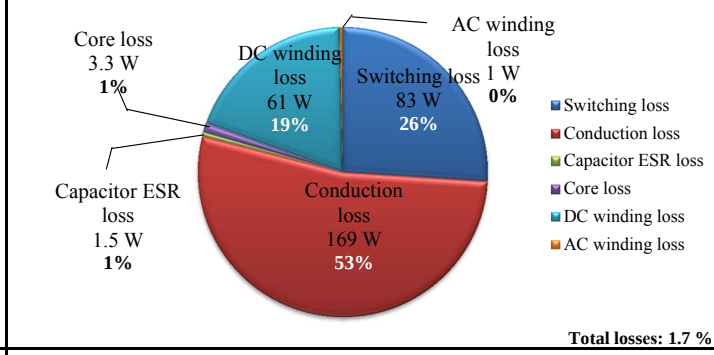
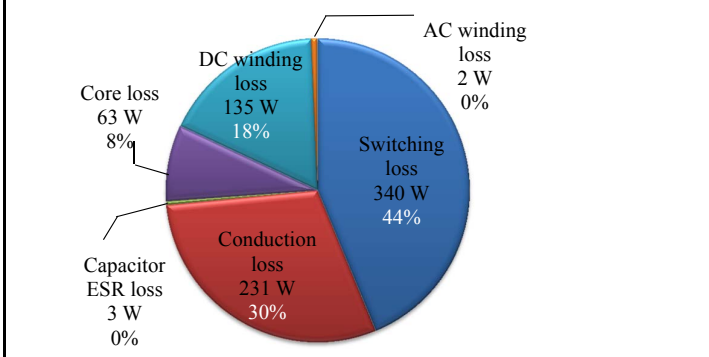
In Fig. 4.12 (b) the generated switch voltage and current at voltage gain four is shown which matches the calculated values of these voltages and currents.

In order to clarify the results shown in Table 4.3, specification parameters of the Boost converter at 20 kW load power and two different voltage gain are listed in Table 4.2. In Table 4.3 a pie chart distribution of different losses is presented at 20 kW rated power and two different voltage gains (2, and 4) for the boost converter. To summarize the previous analysis for the efficiency and loss mapping investigation to be easily compared. The total losses are listed at the bottom right in Table 4.3 which is calculated from the total power loss of the converter by measuring the total efficiency.

TABLE 4.2 Specification parameters for the Boost converter at 20 kW load power and two voltage gain.

Parameters		Value	
		Gain 2	Gain 4
Input voltage	V_{in}	200 V	100 V
Output voltage	V_{out}	400 V	400 V
Duty cycle	D	0.5	0.75
Output power	P_o	20 kW	20 kW
Switching frequency	f_s	20 kHz	20kHz
Inductor	L_{min}	250 µH	93.75 µH
Ripple inductor current	ΔI_L	20 A	40 A
No. of turns	N	64 turns	27 turns
Dc resistance	R_{dc}	0.00624 Ω	0.00347 Ω
Core type		High flux 58337	Metglas AMCC 125
Heat sink		FISHER ELECTRONIK, part no. LA 9/100 230V, 0.28 °C/W	H S MARSTON, part no. 890SP-03000-A-100, 0.04 °C/W
Switch	IGBT rating	**(IXXX200N60C3)** 600 V and 200 A	**(MG06600WB-BN4MM)** 600 V and 600 A
Diode	D_1 rating	**(IDW100E60)** 600V and 100 A	**(DB2F200N/P6S)** 600V and 200 A

TABLE 4.3 Distribution of the different losses for the Boost converter at 20 kW load power and two voltage gain [78].

Gain	Boost converter
Gain 2	
Gain 4	

4.5 Simulation results for the Z-source converter under different power loadings and voltage gains

In this subsection the simulation model of the Z-source converter which is implemented in the PLECS toolbox is shown in Fig. 4.13.

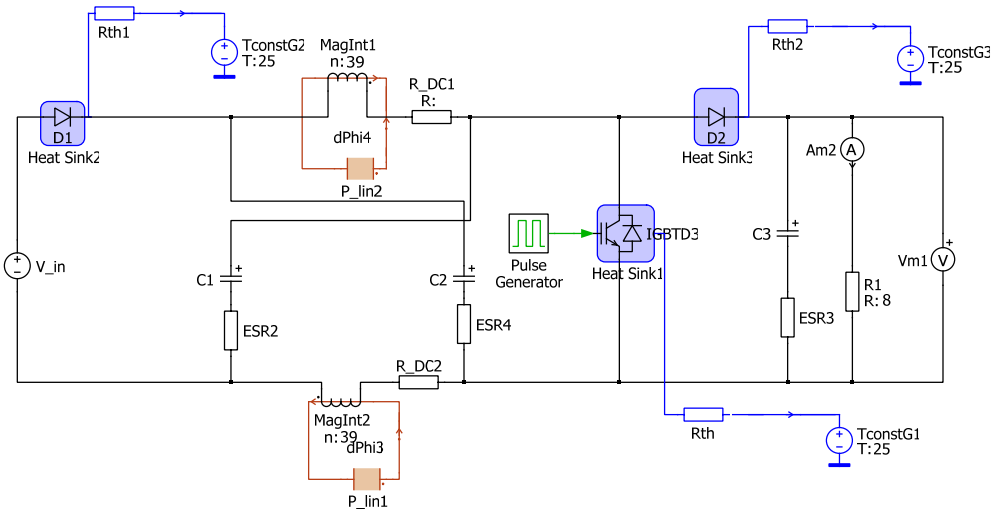


Fig. 4.13: Schematic diagram of Z-source converter in PLECS.

The function blocks shown in this figure are used for the loss mapping analysis as explained earlier in Chapter 3. It consists of a DC source at the input voltage side, two linear magnetic core (L_1 and L_2) with a certain number of turns depending on the calculated inductor value and two capacitors (C_1 and C_2) connected in an 'X' shape.

The semiconductors devices (IGBT, diodes D_1 and D_2) are placed with heat sinks in order to be able to measure the device losses (switching and condition losses) and as well as estimating the junction temperature of the devices. An output capacitor and a resistive load is placed at the output side in order to be able measure the output voltage and the output current through the voltmeter and ampere-meter placed at the output side.

In the the following subsection, some of the obtained waveforms from the simulation model of the Z-source converter are presented under two different voltage gains (2, and 4).

4.5.1 Basic waveforms of Z-source converter using voltage gain 2 and 4

In this subsection, it can be seen than the switch current is almost doubled from voltage gain 2 to 4 and the switch voltage level is the same. In Fig. 4.14 (a) the generated switch voltage and current at voltage gain two is shown. In Fig. 4.14 (b) the generated switch voltage and current at voltage gain four is shown which matches the calculated values of these voltages and currents for both voltage gains.

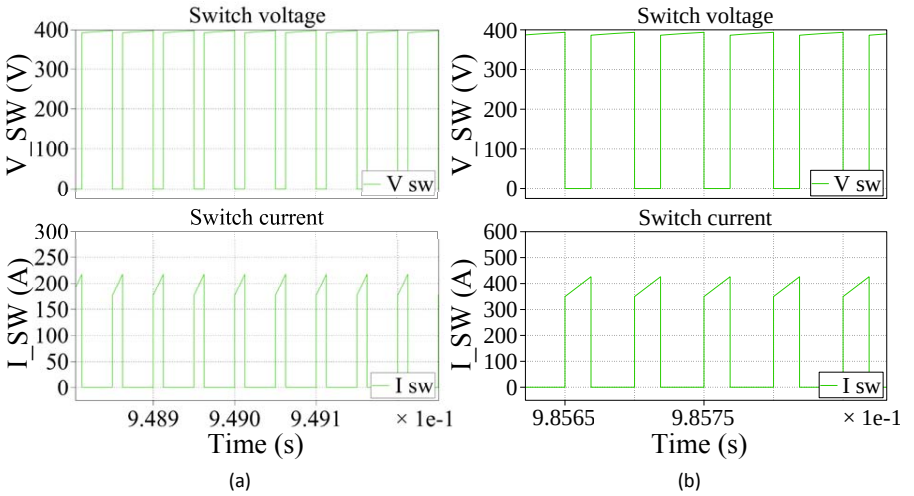


Fig. 4.14: Generated waveforms for the voltage and current across a) Switch using voltage gain 2 b) Switch using voltage gain 4 of the Z-source converter.

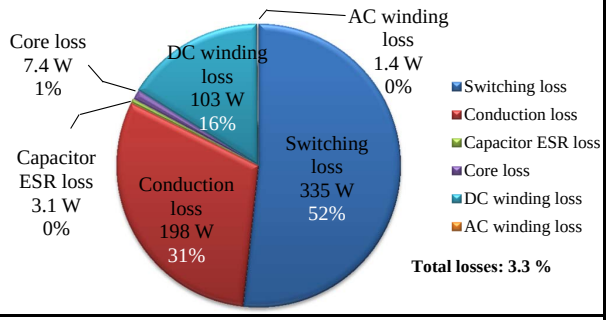
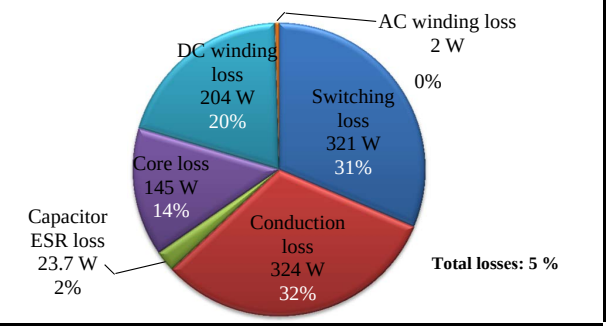
In order to clarify the results shown in Table 4.5, the used parameters of the Z-source converter at 20 kW load power and two different voltage gain are listed in Table 4.4. The switching losses remain almost the same for gain 2 and 4 (unlike the boost converter), due to that two parallel devices were added in the voltage gain of 4. The core losses are much bigger in voltage gain 4, due to that the peak flux density $\hat{B}$ is much higher than in voltage gain of 2 and also it is using different type of core as shown in Table 4.4. In Table 4.5 a pie chart distribution of different losses is presented at 20 kW rated power and at two different voltage gains (2, and 4) for the Z-source converter. To summarize the previous analysis for the efficiency and loss mapping investigation to be easily compared. The total losses listed at the bottom right in Table 4.5 is calculated from the total power loss of the converter by measuring the total efficiency.

4.5. Simulation results for the Z-source converter under different power loadings and voltage gains

TABLE 4.4 Specification parameters for the Z-source converter at 20 kW load power and two different voltage gain.

Parameters		Value	
		Gain 2	**Gain 4**
Input voltage	V_{in}	200 V	100 V
Output voltage	V_{out}	400 V	400 V
Duty cycle	D	0.25	0.375
Output power	P_o	20 kW	20 kW
Switching frequency	f_s	20 kHz	20kHz
Inductor	L_{min}	93.75 µH	117.18 µH
Capacitor C_1 & C_2	C_{min}	208.33 µF	750 µF
Capacitor C_{out}	C_{min_out}	78 µF	117 µF
Ripple inductor current	ΔI_L	20 A	40 A
No. of turns	N	55 turns	30 turns
Dc resistance	R_{dc}	0.00536 Ω	0.0027 Ω
Core type		High flux 58337	Metglas AMCC 160
Heat sink		H S MARSTON, part no. 890SP-03000-A-100, 0.04 °C/W	H S MARSTON, part no. 890SP-03000-A-100, 0.04 °C/W
Switch	IGBT rating	**(MG06400D-BN4MM)** 600 V and 400 A	**(MG06600WB-BN4MM)** 600V and 600 A
Diode D_1	D_1 rating	**(DS1F300N6S)** 600V and 300 A	**(SD600N/R Series)** 600V and 600 A
Diode D_2	D_2 rating	**(DS1F300N6S)** 600V and 300 A	**(DS1F300N6S)** 600V and 300 A

TABLE 4.5 Distribution of the different losses for the Z-source converter at 20 kW load power and two voltage gain [78].

Gain	Z-source converter
Gain 2	
Gain 4	

4.6 Simulation results for the Y-source converter under different power loadings and voltage gains

In this subsection the simulation model of the Y-source converter implemented in PLECS is shown in Fig. 4.15.

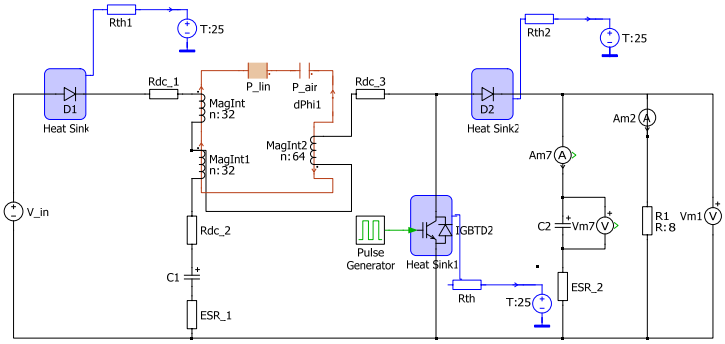


Fig. 4.15: Schematic diagram of Y-source converter used in PLECS.

The function blocks shown in this figure are used in the loss mapping analysis as explained earlier in Chapter 3. It consists of DC source at the input voltage side, the Y-source impedance network with a three-winding coupled inductor (N_1, N_2, and N_3). It has an active switch SW, two diodes (D_1, and D_2). The semiconductors devices (IGBT, diodes D_1 and D_2)are placed with heat sinks in order to be able to measure the device losses (switching and condition losses) and as well as estimating the junction temperature of the devices. An output capacitor and a resistive load is placed at the output side in order to be able measure the output voltage and the output current through the voltmeter and ampere meter placed at the output side.

In the following subsection, some of the obtained waveforms from the simulation model of the Y-source converter is presented under two different voltage gain (2, and 4).

4.6.1 Basic waveforms in Y-source converter using voltage gain 2 and 4

In Fig. 4.16 (a) the generated switch voltage and current at voltage gain two is shown, it can be seen that the switch current is almost triple from voltage gain 2 to 4 and the switch voltage level is the same. In Fig. 4.16 (b) the generated switch voltage and current at voltage gain 4 is shown, which matches the calculated values of these voltages and currents for both voltage gains.

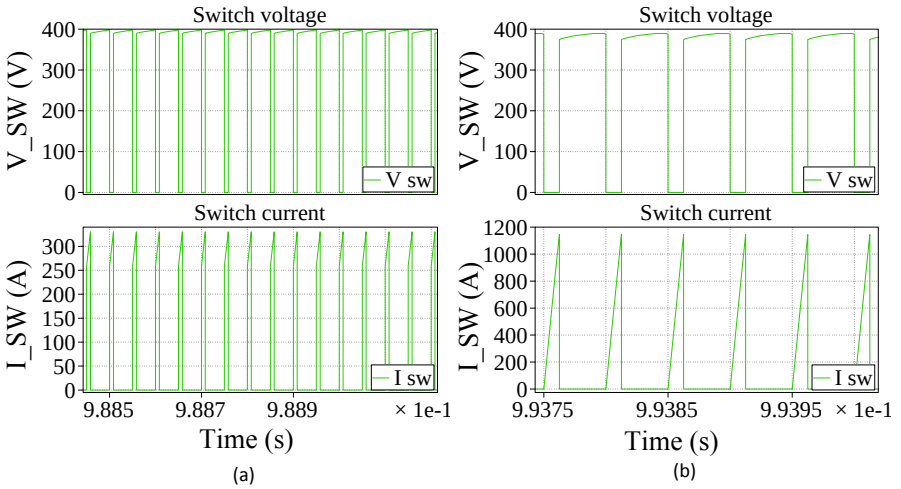


Fig. 4.16: Generated waveforms for the voltage and current across a) Switch using voltage gain 2 b) Switch using voltage gain 4 of the Y-source converter.

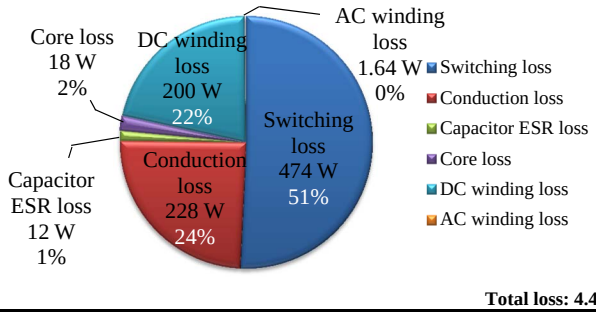
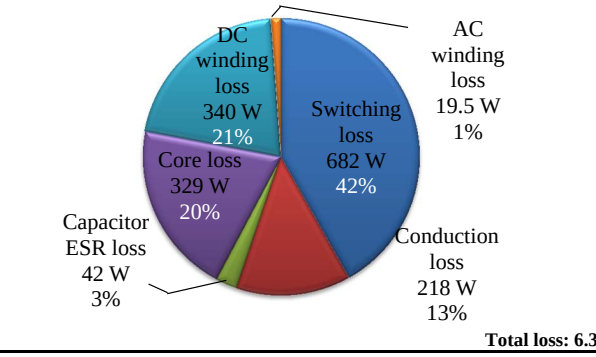
In order to clarify the results shown in Table 4.7, the specification parameters of the Y-source converter at 20 kW load power and two different voltage gains are listed in Table 4.6. The core loss becomes higher for voltage gain 4 than voltage gain 2, due to lower turns ratio and different cores are used as listed in Table 4.6 and also in order to improve the efficiency of voltage gain 4.

TABLE 4.6 Specification parameters for the Y-source converter at 20 kW load power and two different voltage gain.

Parameters		**Value**	
		Gain 2	**Gain 4**
Input voltage	V_{in}	200 V	100 V
Output voltage	V_{out}	400 V	400 V
Duty cycle	D	0.167	0.375
Output power	P_o	20 kW	20 kW
Switching frequency	f_s	20 kHz	20kHz
Inductor	L_{min}	327.86 µH	31.25 µH
Capacitor C_1	C_{min}	63 µF	750 µF
Capacitor C_{out}	C_{min_out}	156.25 µF	234.375 µF
Ripple inductor current	ΔI_L	20 A	120 A
No. of turns	N	32:32:64 turns	7:7:14 turns
Dc resistance	R_{dc}	0.00312, 0.00312 & 0.00624 Ω	0.001, 0.00068, & 0.0015 Ω
Core type		High flux 58337	Metglas AMCC 1000
Heat sink		H S MARSTON, part no. 890SP-03000-A-100, 0.04 °C/W	Hi-Contact Liquid Cold Plates, 0.04 °C/W
Switch	IGBT rating	**(MG06600WB-BN4MM)** 600V and 600 A	**(MG06600WB-BN4MM)** 600V and 600 A
Diode D_1	D_1 rating	**(VSK.9112)** 1200V and 100A	**(SKN 501/12 Semikron)** 1200V and 720 A
Diode D_2	D_2 rating	**(DS1F300N6S)** 600V and 300 A	**(DS1F300N6S)** 600V and 300 A

In Table 4.7 a pie chart is shown to illustrate distribution of different losses at 20 kW rated power and at two different voltage gains (2, and 4) for the Y-source converter. The previous analysis for efficiency and loss mapping can be used for comparison. The total losses listed at the bottom right in Table 4.7 is calculated from the total power loss of the converter by measuring the total efficiency.

TABLE 4.7 Distribution of the different losses for the Y-source converter at 20 kW load power and two different voltage gain [78].

Voltage gain	Y-source converter
Gain 2	
Gain 4	

4.6.2 Junction temperature investigation of the switch using voltage gain 2 and 4

In this subsection, the load power is varying from 1 to 20 kW, and a constant ambient temperature is assumed to be 25 °C. The junction temperature variation of the compared topologies are shown in Fig. 4.17 for voltage gain of 2. Fig. 4.18 shows the junction temperature variation at different loading power for voltage gain of 4.

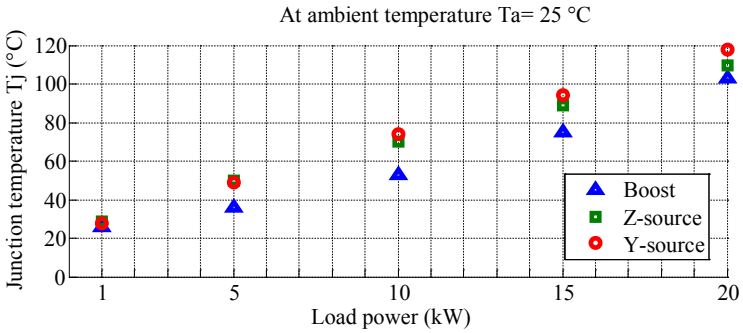


Fig. 4.17: Junction temperature for the switch at different power loading and using voltage gain of 2.

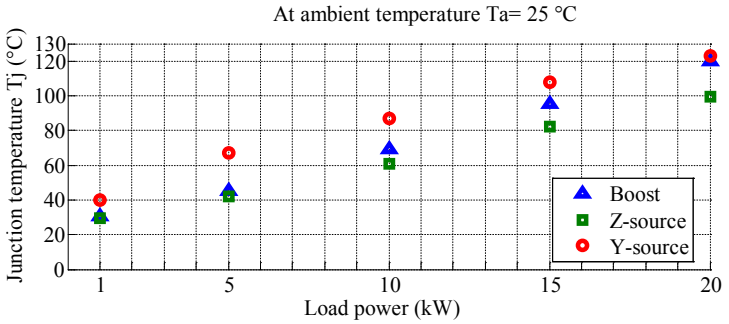


Fig. 4.18: Junction temperature for the switch at different power loading and using voltage gain of 4.

The efficiency is calculated according to the total power losses for each converter as listed in Chapter 3 by using the same conditions as listed earlier. The results in Fig. 4.19 show that the boost converter has the highest efficiency of 98 % compared with the Y-source converter of 96 % and the Z-source converter of 96.7 % at 20 kW loading power. The measured efficiencies from the low power loading (1 kW) to higher power loading (20 kW) is also shown in 4.19. The same analysis is repeated for voltage gain of 4 as shown in 4.20.

In Table 4.8 a comparison of the total efficiencies using voltage gains of 2 and 4 for the compared converters at 20 kW load power.

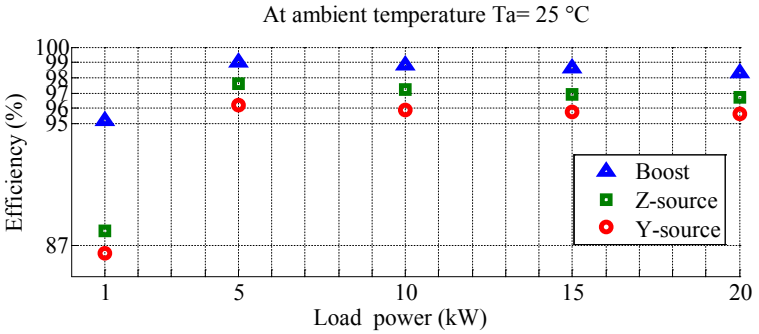


Fig. 4.19: The efficiency at different loading power and using a voltage gain of 2.

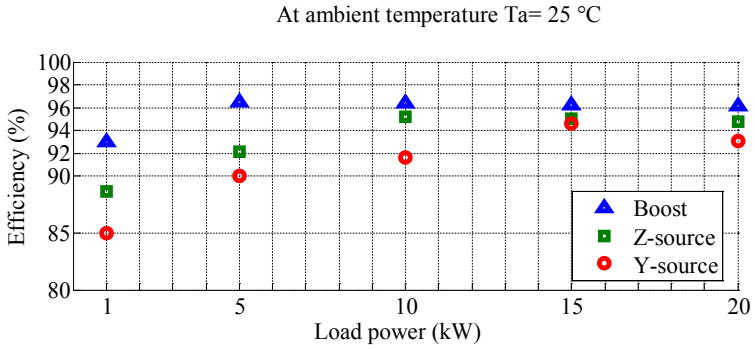


Fig. 4.20: The efficiency at different loading power and using a voltage gain of 4.

TABLE 4.8 Comparison of the total efficiencies using gain 2 and gain 4 for the compared converters at 20 kW load [78].

Efficiency	**Boost converter**	**Z-source converter**	**Y-source converter**
Gain 2	98.3 %	96.7%	95.6%
Gain 4	96.1 %	95%	93.7%

4.7 Summary

In this study different loading conditions between 1 kW and 20 kW are considered during the studies of the efficiency and junction temperature of the converters for two different voltages gain (2 and 4). The results show that the boost converter has higher efficiency than the Z-source and Y-source converter for these specific voltage gains of 2 and 4.

The junction temperature variation in voltage gain of 4 is higher than the junction temperature variation in voltage gain of 2. Investigations on both the magnetic and electrical losses are also given.

The magnetic losses which in the Y-source converter is sharing 34% and 42% of the total losses in voltage gain of 2 and 4 receptivity which is higher than in the boost and Z-source converters.

In the electrical losses it can be noticed that the total electrical loss for voltage gain of 4 is lower than for voltage gain of 2 which clarify that having higher current ratings devices improve the efficiency.

The thermal performances are quite similar in the 3 converters for both voltage gains. The boost converter has better efficiencies in the two selected voltage gains, but it has also the highest decrease in the efficiency from gain 2 to gain 4 at 20 kW power loading compared with the Z-source and Y-source converters.

Chapter. 5

Applied DC/DC Boost Converters in Fuel Cell Applications

5.1 Introduction

Fuel cells are a very promising source of energy since they are pollution free, producing only electricity, water, and heat. It has been a significant force in the development of technology over the past 30 years, and an increasing attention is drawn towards the technology today.

Regardless the size, fuel cells are one of the clean energy and efficient sources. They are also flexible with respect to their physical allocation [80]. In respect to the efficiency, fuel cells are able to operate with the double efficiency of conventional combustion engines [80], [81].

Serenergy's fuel cell (Serenus 166 / 390 Air C) voltage/current characteristic (polarization curve) [82] is used in this study has some advantages such as:

1) Simple, cost-effective, air-cooled fuel cell technology.

2) High fuel flexibility (through use of fuel cell reformer systems).

3) Reliable operation under extreme temperature conditions.

4) High fuel cell system efficiency.

5) Cooling under all environmental conditions.

6) Compact and lightweight fuel cell module design [82].

The polarization curve illustrating the Voltage/Current characteristic is shown in Fig. 5.1

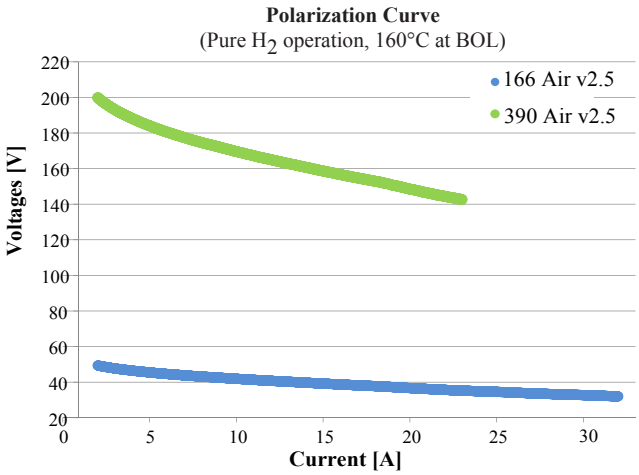


Fig. 5.1: Fuel cell stack module of Serenus 166 / 390 Air C polarization curve [82].

Some of the disadvantages of the fuel cells are that they have lower performance with the ripple current and an output voltage that varies with current and age. For those reasons, power converters are normally used in order to step-up (boost) and regulate the voltage. In addition, they also serve as DC power source [83].

Fuel cells have been applied to DC/DC converters where the reliability and lifetime are some of the high priority performance factors. The ambient temperature is set to 25 °C based on a study in [84] for the lifetime prediction of a fuel cell converter comparing two different cases (India and Denmark) considering the annual ambient temperature mission profiles range from 15 °C to 35 °C as an average value.

A lifetime prediction model is applied for the power semiconductors which are used in the fuel cell DC/DC converters. The common used Coffin-Manson lifetime model and Semikron lifetime model for the IGBTs solder and bond wire fatigues are considered and used to compare in the three designed DC/DC converters where voltage gain 4 is selected using the same switch rating for the three converters, in order to investigate whether the boost converter is efficient any more with higher voltage gain than the two converters as discussed in the previous chapters.

The main component details of the fuel cell hybrid electric vehicle system

is shown in Fig. 5.2 as stated earlier in Chapter 1. It can be seen that the detailed system is consisting of the following models; the fuel cell stack, electric machines, inverters, energy storage devices, and DC/DC converters [19].

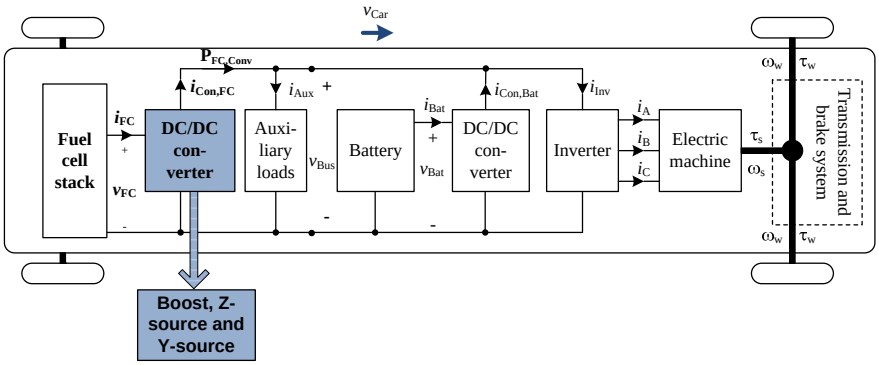


Fig. 5.2: Representation of the Fuell Cell Hybrid Electric Vehicle diagram [19].

In order to estimate the lifetime of the converters a junction temperature mission profile is taken into account to estimate the impact on the IGBTs lifetime during the steady state operation. A case study using "Artemis motorway driving cycle" is considered and applied to the three compared converters in order to fix the application in this analysis. Lifetime consumption and the expected number of years before failure is presented and compared for the Boost, Z-source and Y-source converters. Therefore, a reliability metric as lifetime prediction should be studied for the same compared three converters which are Boost, Z-source and Y-source converters.

In this study the power semiconductors devices are the main component to assess the lifetime of the converters based on the investgation in [78]. There are several lifetime models for power semiconductor devices, and they can be classified into empirical lifetime models used for the characterization of power cycling capabilities of power modules, e.g., the lifetime models presented in [85], [86]. It is the most widely used method for the lifetime prediction of IGBT modules. The main disadvantage of empirical lifetime models is that they are based on statistical analysis of available lifetime data, which do not directly describe the physical failure mechanisms [87].

Other lifetime prediction models are the analytical ones. Analytical lifetime models estimate the life of an IGBT power module in terms of number of cycles to failure considering different factors as temperature swing, average temperature, bond wire current and frequency [87]. The analytical lifetime modelling is combined the use of Palmgren Miner rule. The problem with these models is to accurately identify, extract and count the cycles from the junction temperature profile.

The most commonly used cycle counting method for accurately extracting thermal cycles within the temperature profile is the Rainflow counting analysis. It assumes that each identified thermal cycle produces some degree of damage on the IGBT and thus it contributes to the life consumption of the device [88].

There are different sources of failures in power semiconductor modules and two of the most commonly observed are solder fatigue and bond-wire damage. The power loss variation of the converter will lead to temperature cycling in the device as discussed previously, and the temperature cycling may affect the connections of the solder and the bond wires. When the power cycling and temperature cycling come to a certain number, the solder or the bond wire will wear out. Although different types of semiconductors and converters are used, they share the same lifetime prediction procedure [89].

Furthermore, the load conditions are one of the most dependent factors that affect the lifetime of a power module, since most of the wear out mechanisms are related to the cyclic loading of the module. Therefore, it is necessary to consider the mission profile of the application when estimating the power cycling lifetime of a power module. The power cycling lifetime N_f of a power module is typically given as a function of junction temperature swing amplitude ΔT_j and mean junction temperature T_m.

This chapter apply lifetime prediction models for three types of a DC/DC fuel cell converters based on a driving cycle using Artemis Motorway, and using the generated junction temperature profile of the power module upon operation in order to assess the lifetime of the converters.

5.2 Fuel cell hybrid electric vehicle (FCHEV) system configuration for the reliability analysis

In the fuel cell applications, the power semiconductor devices are exposed to different stresses as thermal stresses due to the load variation behaviour and the ambient temperature as well. The mission profile can be the output power, output current, or the junction temperature profile of the device.

Therefore, a mission profile of 10 repetitions of Artemis Motorway Driving Cycle [90] is applied on a FCHEV based on Toyota Avensis physical parameter as shown in Fig. 5.3 and Fig. 5.4 which shows the speed of the HEV in km/h (driving cycle length = 287.4 km/cycle) presented from the 10 repetitions of Artemis Motorway Driving Cycle.

This driving cycle is the frame work of this investigation. Based on the obtained results shown in Fig. 5.4, Fig. 5.5, and Fig. 5.6 the junction temperature profiles can be defined in the power converter.

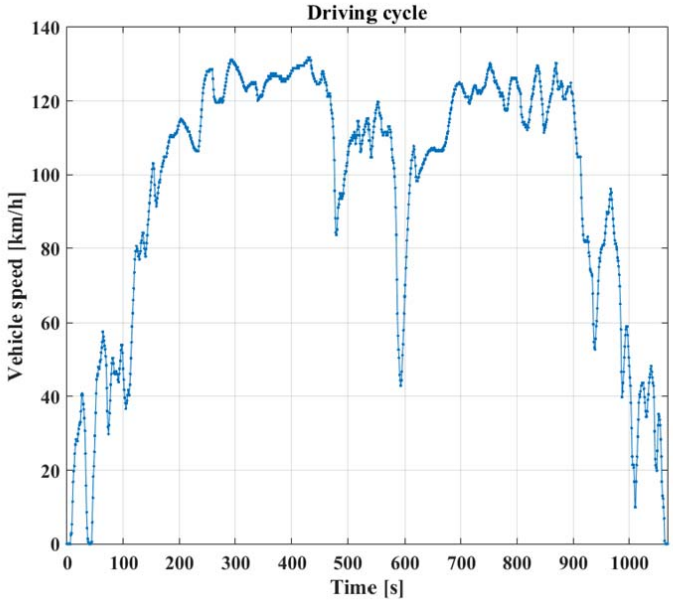


Fig. 5.3: Artemis Motorway Driving Cycle mission profile [90].

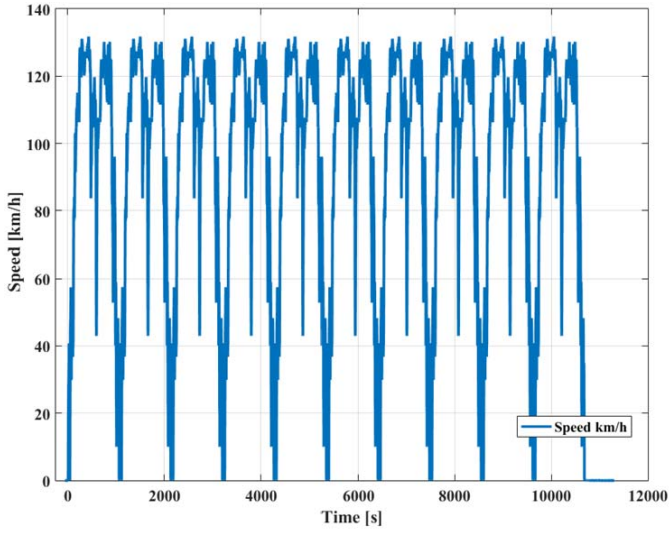


Fig. 5.4: 10 repetitions of Artemis Motorway Driving Cycle presents the speed of the hybrid electric vehicle (HEV) [90].

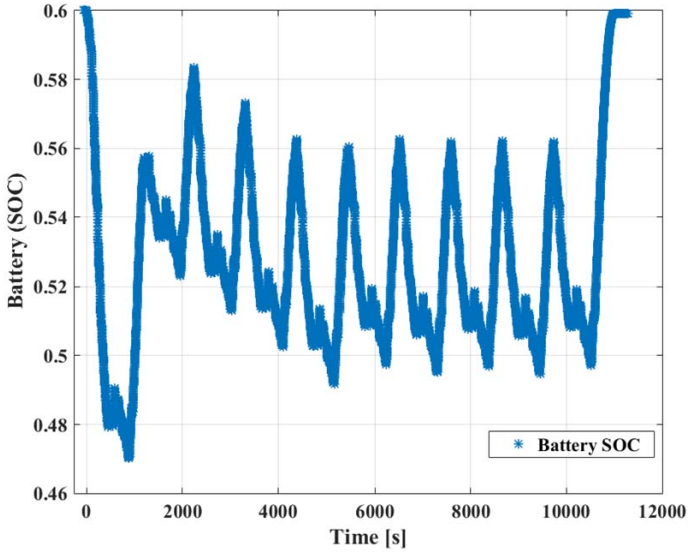


Fig. 5.5: The state of charge (SOC) of the converter battery.

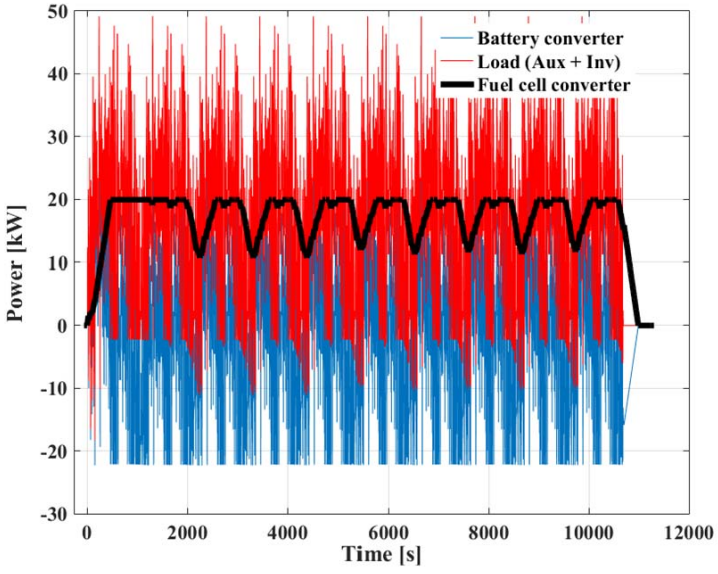


Fig. 5.6: The fuel cell converter power, the converter battery and the load.

The operation of a Hybrid Electric Vehicle is presented in Fig. 5.5 which shows the converter fuel cell power, the battery converter and the load and Fig. 5.6 which shows the state of charge (SOC) of the battery. The fuel cell follows the load with low dynamic power production and the battery acts as a buffer.

5.3 Lifetime modelling for fuel cell converters

In this section, based on the previously mentioned loss evaluation in Chapter 3, the IGBT module is the most stressed component in the converter fuel cell [78] seen from the junction temperature profile. The process of lifetime estimation is shown in Fig. 5.7.

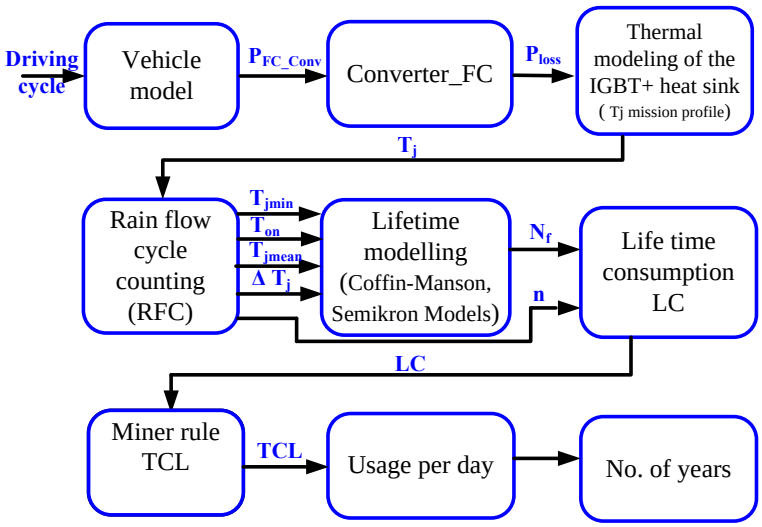


Fig. 5.7: Process to estimate lifetime of the IGBT module in years.

It starts with the vehicle modelling and it is an input of 10 repetition of Artemis Motor way driving cycle (*Driving cycle*), output of the fuel cell converter (P_{FCconv}) is the output from the vehicle model, fuel cell converter power loss profile (P_{Loss}) and thermal modelling of the IGBT module for extracting the junction temperature profile (T_j). Applying the Rainflow counting algorithm to count the cycles with their minimum and mean junction temperature, pulse duration and the counted number of cycles to failure (T_{jmin}, T_{on}, T_{jmean}, and ΔT_j). The lifetime modelling is the next step in order to get the cycles to failure and its counted number (N_f, and n), and finally calculate the consumed life (LC), then Miner rule is applied to find total consumed life

(TCL) and according to the usage per day based on (5.7) the estimation for the number of years seen before failure is calculated.

As shown in Fig. 5.7 which present the process of the lifetime estimation, the Rainflow counting (RFC) algorithm is one of the common steps used to predict the lifetime of the IGBT module. RFC has been one of the most popular cycle counting techniques used in fatigue analysis. A Rainflow code is programmed, where it divides the input curve into t_{sim} (simulation time), T_j (junction temperature readings) and ΔT_j (cycle amplitude). It is decide that a resolution of ΔT_j = 0.36 $^{\circ}C$ is used in order to consider also the small amplitudes of the cycle fatigue in the junction temperature profile.

5.3.1 Failure mechanisms during the power cycling

In a power cycling test, components are actively heated up by the losses in the semiconductor and cooled down again with the aid of cooling equipment. The exposure to this temperature changes leads to the thermo-mechanical stress between the material layers of the module. Therefore, some of the most common failures with the power cycling are the solder fatigue in the chip soldering and the bond wire fatigue [34]. In the solder fatigue, the thermo-mechanical stress leads to an increase in the thermal resistance R_{th} and the chip temperature, which gives higher losses and therefore a higher temperature difference ΔT.

In the bond wire fatigue, which mostly appears with the solder fatigue of the chip, where it is of longer life than the solder fatigue, due to the parallel positioned of the bond wires inside the chips. Thus, the loss of a bond wire will not immediately result in a component failure. But the parallel bond wires should carry additional current, which means that it is not fully destroyed. Afterwards, the bond feet will be heated even more and eventually the chip will be destroyed at the instant of bond wire lift off [91]. Consequently the failure of the component depends on the load and the cooling conditions.

The number of power cycles N_f before failure can be calculated through specific lifetime models, Coffin-Manson lifetime model which is one of the common used model in lifetime prediction for the IGBT modules solder fatigue [92] as given in (5.1):

$$N_f = A.\Delta T_j^{\beta_1}.exp\left(\frac{\beta_2}{T_{jm}+273}\right).t_{on}^{\beta^3}, \tag{5.1}$$

where ΔT_j is the junction temperature swing, T_{jm} is the mean junction temperature, and t_{on} is the cycle on-time duration. The constant parameters A, β_1, β_2, *and* β_3 are provided by the manufacture according to the test data performed [91].

Another lifetime model, which especially focuses on the bond wire fatigue [93]. The number of cycles to failure N_f would be the best calculated if the lifetime model considers the same testing conditions as the ones in the field operation. However, it is almost not feasible in practice due to the required time for testing. The LESIT curves [91] consider the effect of the mean temperature and the temperature level when the temperature cycling takes place. Although many test results indicate that other parameters, such as pulse duration t_{on} and the current amplitude I_B will influence the test results just as much as packaging parameters such as bond wire thickness, chip and solder thicknesses.

In [94] an extended model based on the analysis of a large number of tests is given in (5.2):

$$N_f = A.\Delta T_j^{\beta_1}.exp\left(\frac{\beta_2}{T_{jmin}+273}\right).t_{on}^{\beta 3}.I_B^{\beta_4}.V_C^{\beta_5}.D^{\beta_6}, \tag{5.2}$$

where ΔT_j is the junction temperature swing, T_{jmin} is the minimum junction temperature, t_{on} is the pulse duration and it is assumed to be half the cycle duration for simplicity, I_B is the current per bond foot, V_C is the voltage class/100, and D is the bond wire diameter in μm. The constant parameters A, β_1, β_2, β_3,β_4, β_5, *and* β_6 are given in [91] according to the test data performed and they are listed in the Table 5.1.

TABLE 5.1 Parameters and cofficient used in Coffin-Manson and Semikron lifetime model [89].

A	$\boldsymbol{\beta_1}$	$\boldsymbol{\beta_2}$	$\boldsymbol{\beta_3}$	$\boldsymbol{\beta_4}$	$\boldsymbol{\beta_5}$	$\boldsymbol{\beta_6}$
2.03E+14	-4.416	1285	-0.463	-0.716	-0.761	-0.5

Further, the consumed life CL according to Miner's rule [95] linear fatigue model, the failure occurs when the sum of cycles stress at different magnitudes of n with respect to their corresponding number of cycles to failure N_f reaches one (i.e. LC = 1). Thus the consumed lifetime per cycle amplitude i is given in (5.3) as:

$$CL_{(i)} = \frac{n_{(i)}}{N_{f(i)}}, \tag{5.3}$$

where $n_{(i)}$ is the number of cycles of amplitude i, and $N_{f(i)}$ is the corresponding cycle to failure of amplitude i.

The total consumed lifetime TCL is calculted based on the Miner's rule [95] assuming the linear damage accumulation given in (5.4):

$$TCL = \sum_{i}^{I} CL_{(i)}, \tag{5.4}$$

which means the summation of the consumed lifetime as listed in (5.3).

The number of cycles to failure has been calculated based on (5.1) and (5.2) considering the load variations with respect to the mission profile. The junction temperature response is extracted from the mission profile for each load variation. It is worth to mention that both lifetime consumption models are considering the crack in the solder fatigue and the end-of life of the bond wires [91], [92].

5.4 Lifetime estimation based on junction temperature mission profile

5.4.1 Temperature modelling and estimation of the junction temperature of the fuel cell converters

Simple thermal equations are typically used to calculate the junction temperature in steady state as given in (5.6). PLECS simulation tool is used in estimating the junction temperature T_j depending on the thermal description of the devices as given in the data sheet known as the thermal resistance R_{th}.

Calculating the R_{th-ja} ($^{\circ}C/W$) of the device as earlier discussed in Chapter 3 and assuming an ambient temperature of 25 $^{\circ}C$ allows to estimate the rise of the junction temperature inside the devices as in :

$$\Delta T_{Device} = P_{loss} \times R_{th-ja}, \tag{5.5}$$

where ΔT_{Device} is the rise in the device temperature, P_{loss} is the total power loss generated from the device, and R_{th-ja} is the junction to ambient thermal impedance.

$$T_j = \Delta T_{Device} + T_a, \tag{5.6}$$

where T_j is the device junction temperature, and T_a is the ambient temperature.

Based on the previous calculations, the mission profiles of the junction temperature of the converters fuel cell are obtained with respect to the driving cycle of the HEV. These profiles are presented in the next subsection with a comparison of the results for the lifetime estimation.

5.4.2 Comparison for the three fuel cell converters lifetime estimation results

Based on the previous analysis discussed in sections (5.2) and (5.3), the three DC/DC boost converters are applied for the same fuel cell hybrid electric vehicle application, and the same technique for the cycle counting (RFC algorithm) are used and compared with respect to the following:

1) Coffin-Manson lifetime model for solder fatigue

2) Semikron lifetime model for bond wire fatigue.

Assuming a constant ambient temperature of 25 $^{\circ}C$, and the mission profiles are repeated once per day MP_{day} (10 repetition of driving cycle of Artemis Motorway Drive mission profile). The number of years can be calculated in (5.7):

$$\text{No. of years} = \frac{1}{\left(TCL \times MP_{day} \times DY\right)} \tag{5.7}$$

where TCL is the total consumed life per IGBT module, MP_{day} is the no. of repeated mission profiles per day, and DY is the no. of days per year (i.e DY = 365 days).

As shown in Fig. 5.8, Fig. 5.9, and Fig. 5.10 the achieved junction temperature mission profiles for each converter is presented. In each figure that the blue curve is the generated junction temperature via the IGBT module from the converter simulation model, the black dashed line is the input to the RFC- program with a resolution of 0.36 $^{\circ}C$, and the red diamond shaped is the minimum temperature representation per cycle.

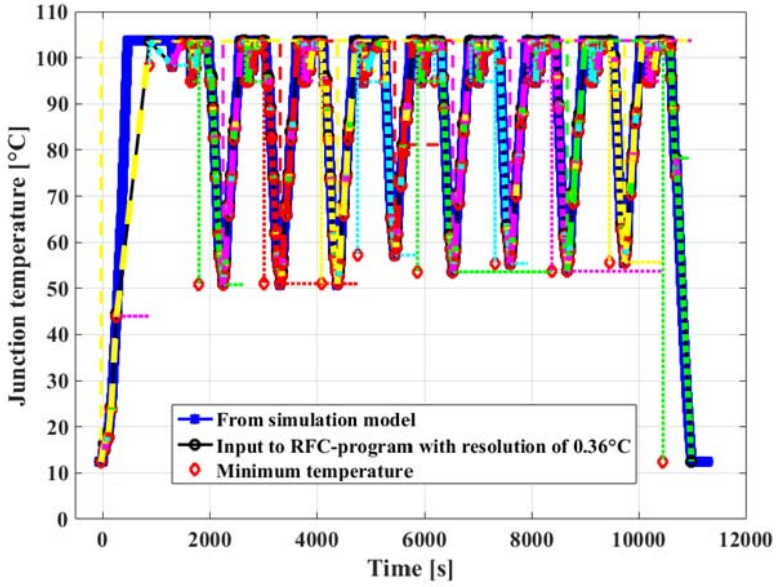


Fig. 5.8: Rainflow counting of the junction temperature profile of the IGBT module in the Boost converter.

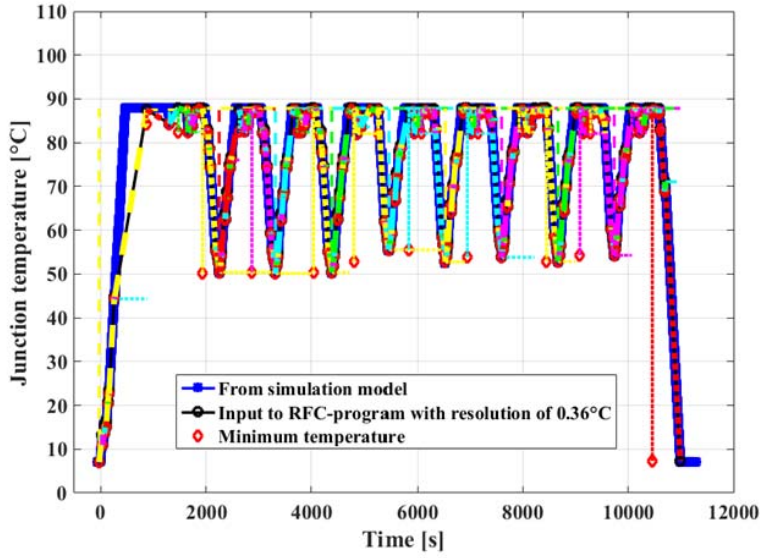


Fig. 5.9: Rainflow counting of the junction temperature profile of the IGBT module in the Z-source converter.

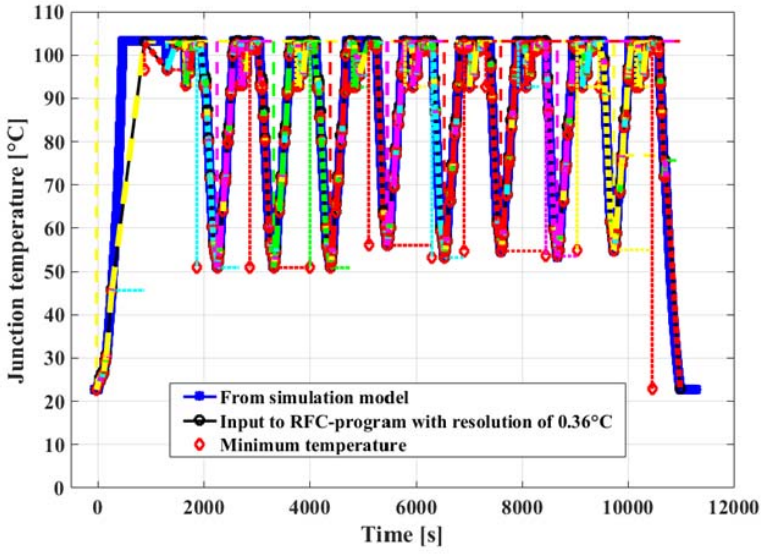


Fig. 5.10: Rainflow counting of the junction temperature profile of the IGBT module in the Y-source converter.

For more detailed analysis of the achieved junction temperature profile of the converters RFC results, Fig. 5.11, Fig. 5.12, and Fig. 5.13 are presented.

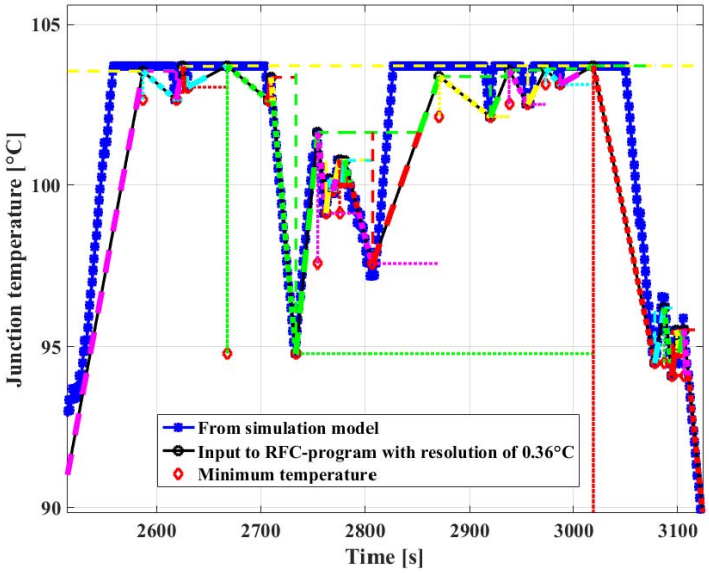


Fig. 5.11: Rainflow counting of the junction temperature profile of the IGBT module in the Boost converter zoomed in.

In Fig. 5.11, RFC of the junction profile of the IGBT module in the Boost converter is zoomed in, in order to be easy to track the counting algorithm of the path of the rain drops down the roof which can be seen for example with the pink path in Fig. 5.12 and more zoomed in is shown in Fig. 5.13.

Moreover, in Fig. 5.14 and Fig. 5.15 the reason for the selection of a resolution of 0.36 $^{\circ}C$ is shown. In Fig. 5.14, it can be seen from the black line which represent input of the RFC- program with a resolution of 0.36 $^{\circ}C$ is able to count most of the small cycle amplitudes.

In Fig. 5.15, the same mission profile is achieved but with a resolution of 2.5 $^{\circ}C$ where it can be obviously seen from the black line is that not all the cycle amplitude is taken in consideration.

Further, the obtained results from the RFC- program is then analysed for the three converters. The results of the boost converter is shown in Fig. 5.16, Fig. 5.17, and Fig. 5.18 respectively.

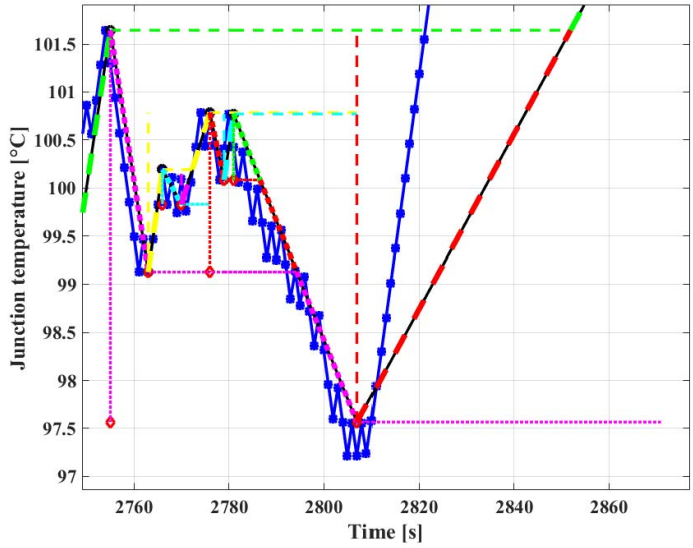


Fig. 5.12: Rainflow counting of the junction temperature profile of the IGBT module in the Boost converter cycle path zoomed in.

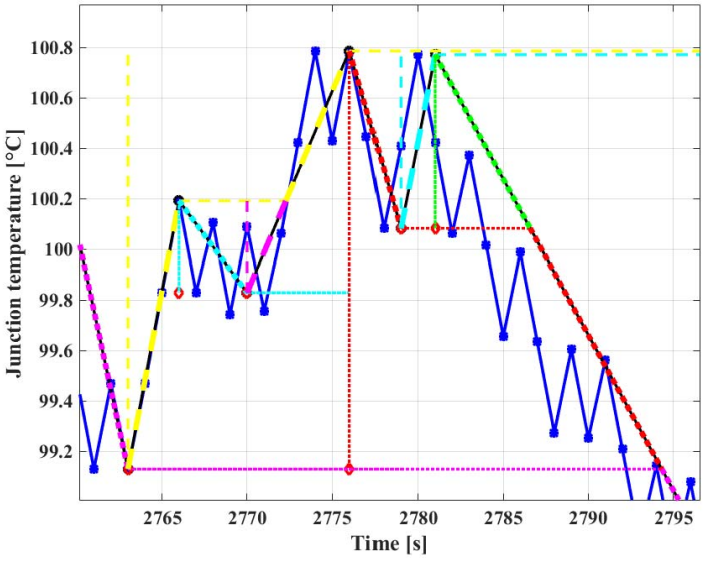


Fig. 5.13: Rainflow counting of the junction temperature profile of the IGBT module in the Boost converter more zoomed in.

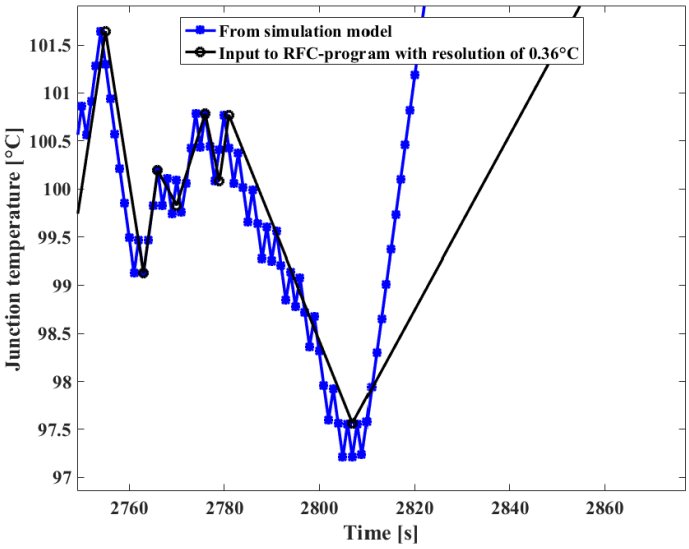


Fig. 5.14: The junction temperature profile of the IGBT module applied to the RFC-program with resolution of 0.36 °C.

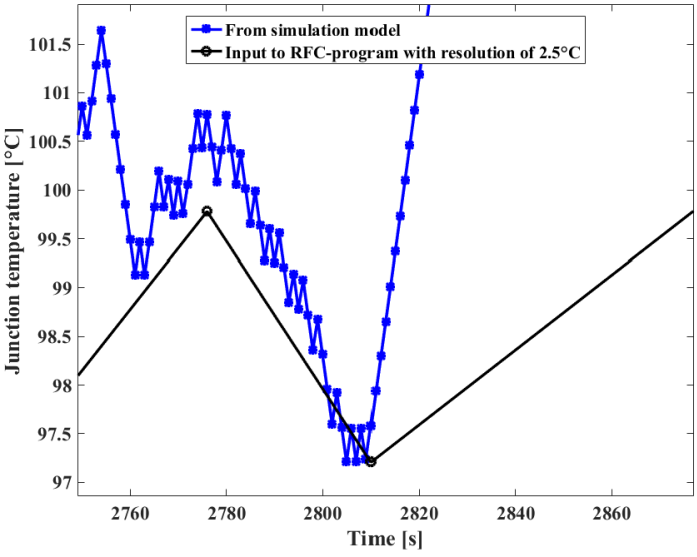


Fig. 5.15: The junction temperature profile of the IGBT module applied to the RFC-program with resolution of 2.5 °C.

In Fig. 5.16, the junction temperature cycle amplitude (cycle depth) based on the resolution of 0.36 $^{\circ}C$ with respect to the number of full cycles is shown.

It can be seen that there are three different levels of the junction temperature cycle amplitude, where the most of the high full cycle counts are found in the range between (0 and 10 $^{\circ}C$). A medium amplitude is seen in another range with a cycle amplitude higher than of (10 to 70 $^{\circ}C$). The last lowest full cycle counts is shown in the range for higher than 70 $^{\circ}C$.

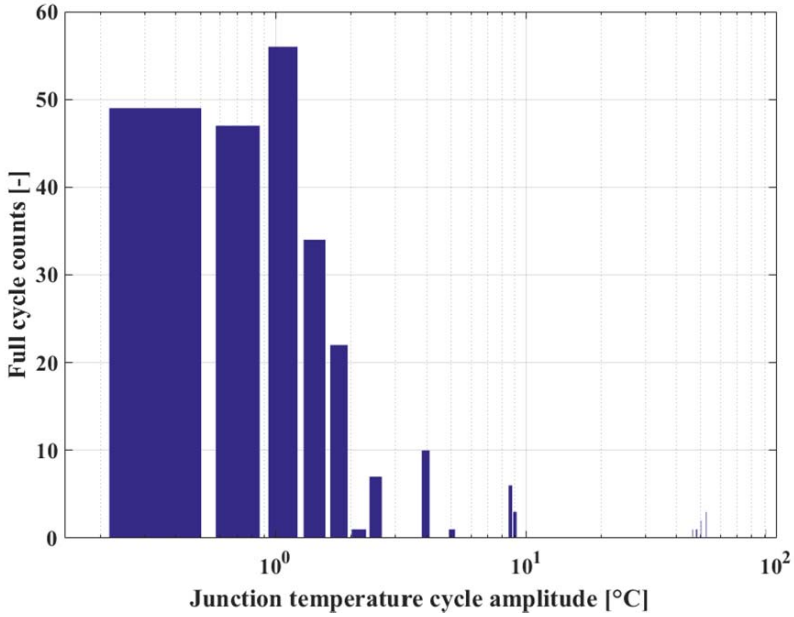


Fig. 5.16: Boost converter junction temperature cycle amplitude with respect to full cycle counts.

In Fig. 5.17, four different plots for the junction temperature cycle amplitude ΔT_j, the minimum value of the junction temperature T_{jmin}, the half cycle pulse duration T_{on}, and the total consumed life TCL all versus the number of half cycles which counts 490 cycles.

In Fig. 5.18, the histogram of the 3D plotting of the three main criterias in this analysis, the number of half cycles, the junction temperature cycle amplitude ΔT_j, and the minimum value of the junction temperature T_{jmin} which obtained based on the RFC- program highest range is from (50 to 110 $^{\circ}C$).

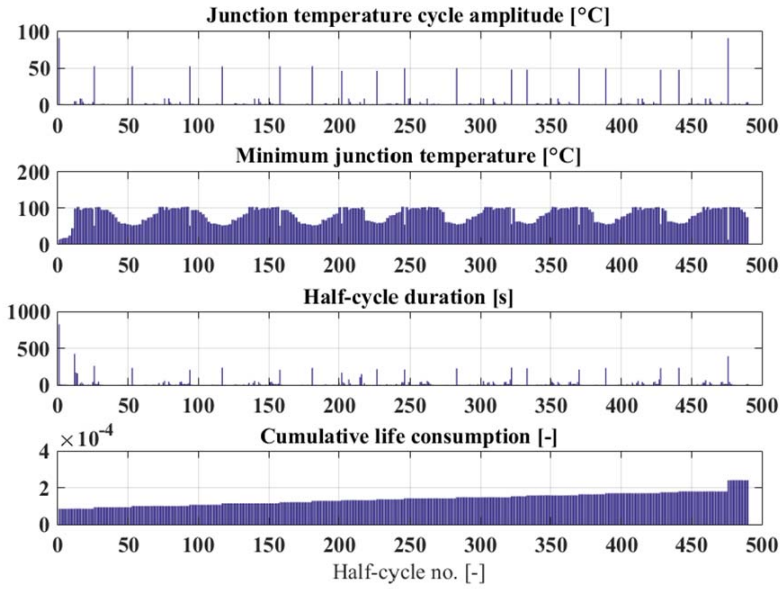


Fig. 5.17: Boost converter where ΔT_j, T_{jmin}, T_{on} and TCL with respect to half cycle counts

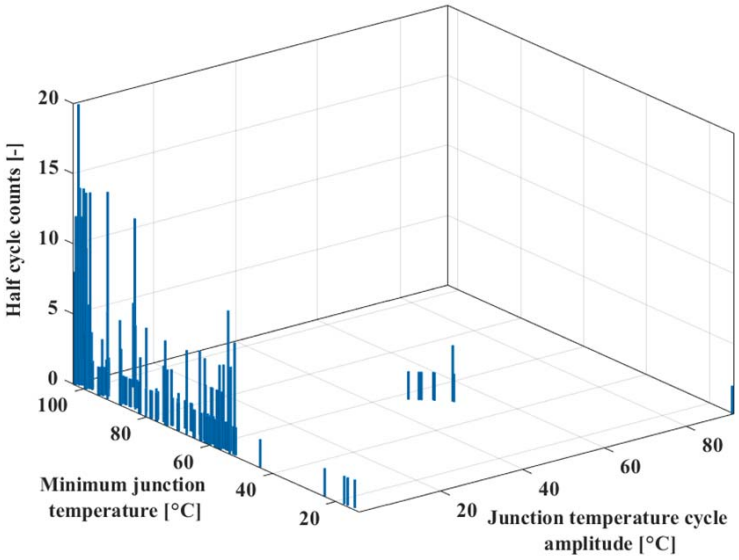


Fig. 5.18: Boost converter half cycle count with respect to T_{jmin} and ΔT_j.

The same analysis is applied to both Z-source and Y-source converters, in Fig. 5.19, Fig. 5.20, Fig. 5.21, Fig. 5.22, Fig. 5.23, and Fig. 5.24 respectively.

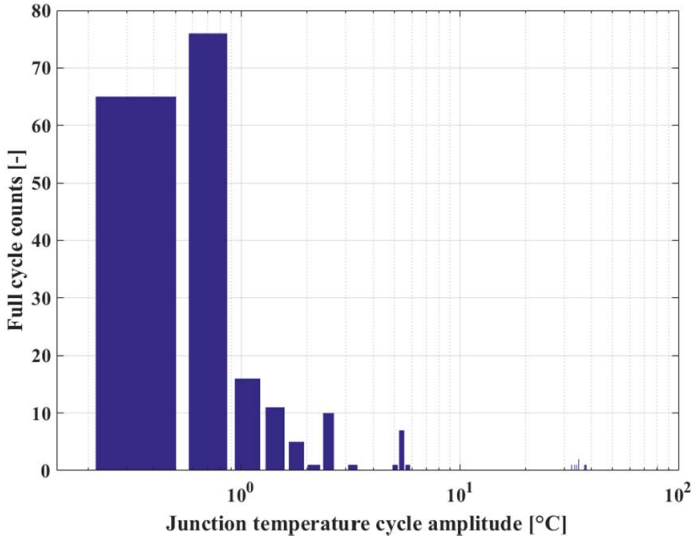


Fig. 5.19: Z-source converter junction temperature cycle amplitude with respect to full cycle counts.

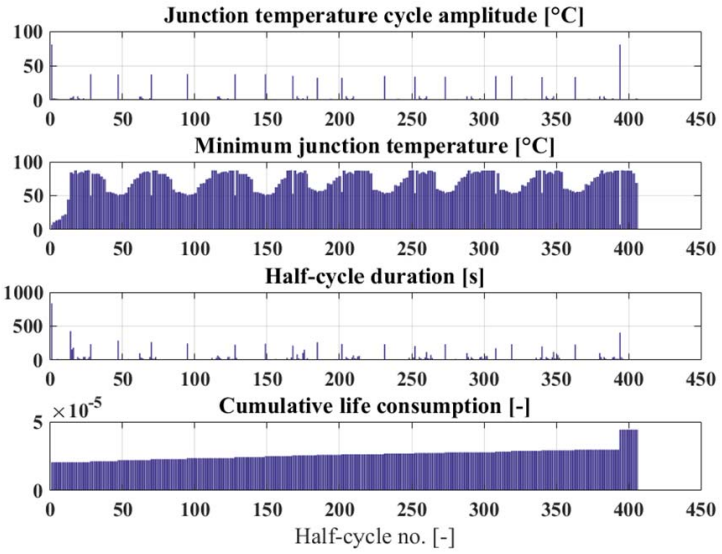


Fig. 5.20: Z-source converter where ΔT_j, T_{jmin}, T_{on} and TCL with respect to half cycle counts

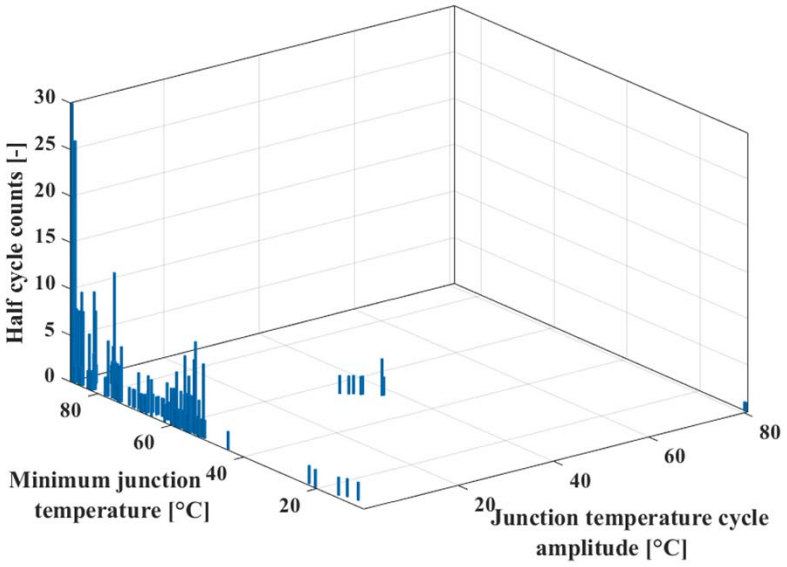


Fig. 5.21: Z-source converter half cycle count with respect to T_{jmin} and ΔT_j.

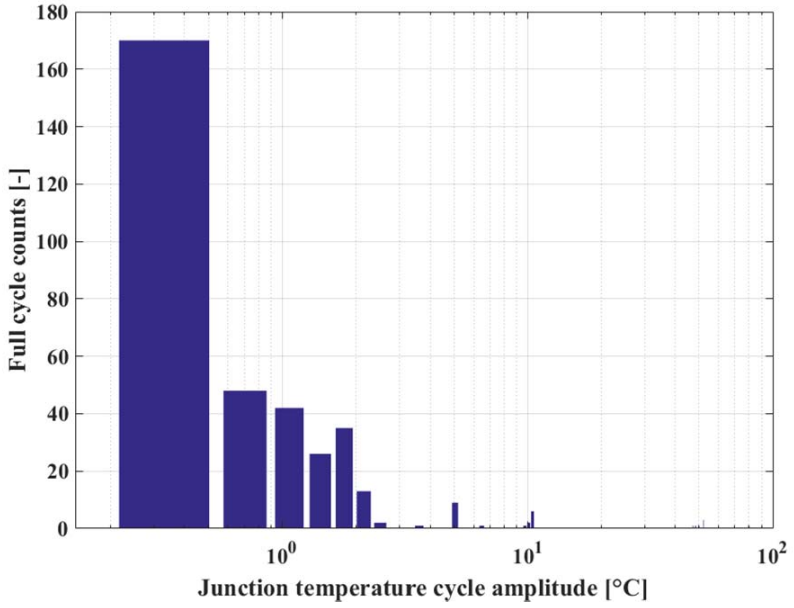


Fig. 5.22: Y-source converter junction temperature cycle amplitude with respect to full cycle counts.

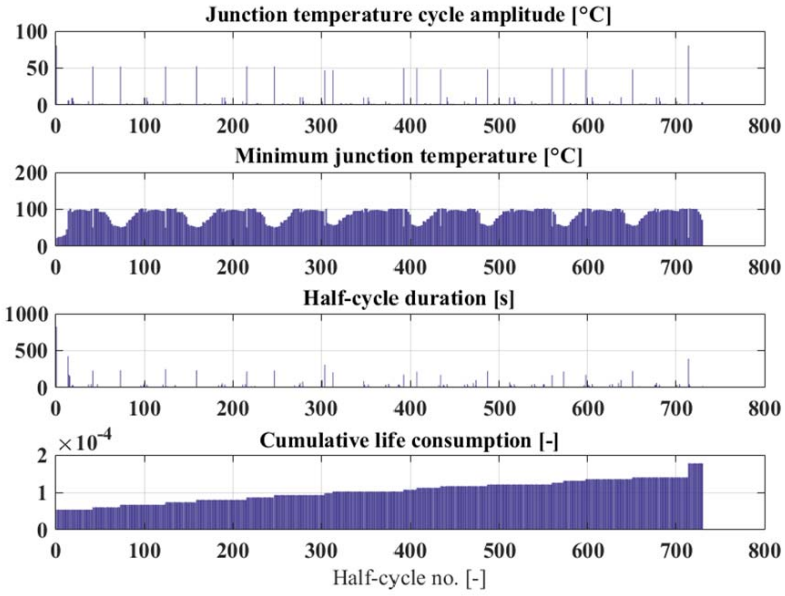


Fig. 5.23: Y-source converter where ΔT_j, T_{jmin}, T_{on} and TCL with respect to half cycle counts.

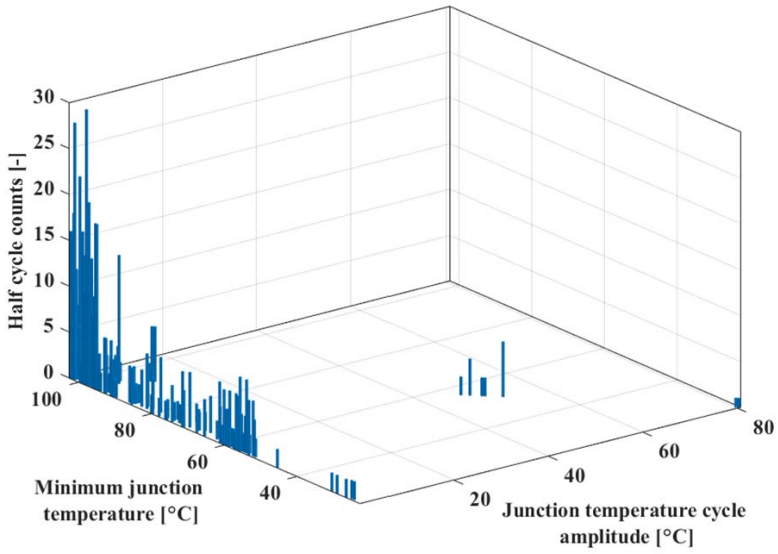


Fig. 5.24: Y-source converter half cycle count with respect to T_{jmin} and ΔT_j.

It can be seen from Fig. 5.20 and Fig. 5.23 that they can be distinguished in the same 3 intervals (high, medium, and low) but with different full cycle

count. The number of half cycles count is 406 cycles in the Z-source converter and 730 cycles in the Y-source converter. In Table 5.2 a summary for the lifetime estimation in years and the total consumed life of each mission profile of the three DC/DC boost converters based on the lifetime models using Coffin-Manson and Semikron models for the solder and bond wire fatigues, respectively.

TABLE 5.2 Lifetime estimation for the three power converters used in fuel cell based electric vehice.

		Boost	Z-source	Y-source
Coffin-Manson Model **(Solder fatigue)**	Life consumption LC_MP	**78.5e-6**	**32.147e-06**	**61.454e-6**
	Expected lifetime in years	**35 years**	**85 years**	**44 years**
Semikron Model **(Bond wire fatigue)**	Life consumption LC_MP	**174.84e-6**	**67.431e-06**	**129e-6**
	Expected lifetime in years	**16 years**	**40 years**	**21 years**

It can be seen that the estimated number of years is higher than the average lifetime of the fuel cell converter, which typically is five to ten years [96]. Due to the fact that the analysis for estimating the lifetime of the converters is only assessing one component, which is the IGBT module, an increased number of years than the average lifetime of the fuel cell converters can be expected since not all the system configuration is assessed. The results show that the Z-source converter has the longest lifetime estimated than the other two converters, due to its lowest maximum junction temperature profile and the lowest cycle to failure counts, which reflects that the total consumed life is the lowest compared to Boost and Y-source converters. The obtained results indicates also that the total driving distance for the HEV is 105,000 km/year, based on that the speed of the vehicle is achieved from 10 repetitions of Artemis Motorway Drive mission profiles where the mission profile MP_{day} is repeated only once per day.

5.5 Summary

In this chapter two different methods to predict the lifetime of power semiconductors for DC/DC fuel cell converters are presented. An Artemis Motorway Drive mission profile is taken into consideration as a frame base of the analysis.

Three DC/DC fuel cell converters (Boost, Z-source and Y-source converters) are designed for 20 kW rated power at gain 4. The IGBT modules are the only assessed component in this investigation, and thus the lifetime of the converters are predicted. Solder and bond wire fatigues are analysed through two lifetime models (Coffin-Manson and Semikron). A rainflow counting algorithm is performed in order to count the cycles to failure for both lifetime models. Junction temperature profiles are the main criteria upon which the lifetime of the converters are decided. The same condition is applied for the three compared converters but separately designed according each converter requirements.

The results shows that Z-source converter basically has a longer lifetime in both lifetime models than the other two converters (Boost and Y-source converters) for the same fuel cell application due to its lowest maximum junction temperature profile and cycle count. It can also be concluded from this analysis that the bond wire fatigue is more critical than the solder fatigue seen from the lifetime estimation.

Chapter. 6

Conclusions

This chapter summarizes the work and concludes the main contributions presented in the thesis based on the obtained results. Finally, future work is added in the last section.

6.1 Summary

The scope of this thesis is presented in Chapter 1, which is divided into several sections which includes the background of the reliability engineering of power electronics, its state of the art, sources of failure in power electronics, components failure and also different life time prediction methods. Moreover, a general description of the system configuration of the fuel cell hybrid electric vehicle (FCHEV) using the Artemis Motorway driving cycle which is used for the analysis in Chapter 5. Then, the thesis structure is presented in order to give a better understanding about the flow of this research work.

Three existing types of boost converters are the frame work of the investigation through this Ph.D. project, which are the Conventional Boost, Z-source and Y-source converters. These types of boost converters are essentially needed in many applications. The basic design, operational principle, mathematical derivations and parameters selection are presented. Advantages for each topology is given, taken into consideration a study and a comparison with their thermal performances of the semiconductors device which indirectly will affect their reliability assessment and efficiency. This investigation is aiming to improve the reliability of the applied FCHEV application from the expected lifetime point of view.

Chapter 3 focuses on the power losses evaluation of the boost type power

converter. The electrical losses (switching and conduction losses), and magnetic losses (inductors) and the capacitor losses are modelled. Thermal modelling is based on the design of the heat sink, temperature modelling of the semiconductor devices and the junction temperature estimations. Each converter is designed separately based on the required ratings and specifications having the same variation of the power loading and voltage gains.

On the basis of the studied DC/DC boost converters, loss distribution, and thermal evaluation of the semiconductors obtained from Chapter 2 and Chapter 3, Chapter 4 further gives a fair and realistic comparison between three different topologies, where PLECS is used for the three converter analysis. Simulation results of the three compared topologies at different voltage gains and power levels is presented. The validation of the Y-source converter is performed by a 300 W rated prototype converter since it is the most recent topology compared to the other two converters. The analysis in this chapter concludes that boost converter has higher efficiency than the Z-source and Y-source converter for specific voltage gains of 2 and 4. A maximum junction temperature of 125 °C has been used as a design constraint for the heat sink. The estimation of the junction temperature of the switches are based on the thermal model and the mapped losses using PLECS. The load power is varying from 1 to 20 kW, and a constant ambient temperature is assumed to be 25 °C. The efficiency is calculated according to the total power losses for each converter as discussed in the Chapter 3. Finally a comparison of the total efficiencies using the voltage gains of 2 and 4 for the compared converters at 20 kW load power is given.

Chapter 5 addresses the evaluation of the fuel cell DC/DC converters (Boost, Z-source and Y-source converters), which are designed for 20 kW rated power and their reliability are assessed based on the lifetime prediction of each converter. The FCHEV system configuration is presented to do the reliability analysis based on Artemis Motorway driving cycle generated from Toyota Avensis hybrid vehicle parameters. The IGBT modules are the only assessed components in this investigation, and based on that the lifetime of the converters is predicted. Two different methods are used to predict the lifetime of the power semiconductors, describing the solder and bond wire fatigues by using two lifetime models (Coffin-Manson and Semikron). The concepts of the consumed lifetime per year and total consumed lifetime are introduced. The rainflow counting algorithm is performed in order to count the cycles to failure for both lifetime models. The junction temperature profiles are the main criteria upon which the lifetime of the converters are decided. The same condition is applied for the three compared converters, but they are separately designed according to each converter requirements. The chapter conclude that the Z-source converter basically has a longer estimated lifetime than the other two converters (Boost and Y-source converters) for the same fuel cell application due to its lowest maximum junction temperature

profile and lower cycle count. It can also be concluded from this analysis that the bond wire fatigue is more critical than the solder fatigue.

6.2 Main contributions

In this thesis, following contributions from the author's point of view can be highlighted:

- Review of the existing reliability assessment methods for power electronics in electro-mobile applications, like sources of failure, components failures as well as different lifetime prediction methods.

  Based on that review, it's decided to start the analysis of the thermal behaviour of the fuel cell hybrid electric vehicles for DC/DC boost converters assessing their reliability from a thermal perspective point of view and determining the estimated lifetime of the converter.

- Design some of the existing DC/DC boost converters (Boost, Z-source and Y-source) upon understanding the basic theory of operation and their circuitry, while having common specification parameters using PLECS to verify the losses modelling of these converters in a simulation model.

- Modelling of all the relevant power losses and do thermal design of the three boost converters, where analytical equations are used and verified by simulation models using PLECS. Temperature modelling is also included in order to estimate the junction temperature profiles for the assessed components (IGBT module) at different power loading and different voltage gains.

- Validation of the Y-source converter at 300 W rated power.

- Generating the junction temperature profiles for the IGBT modules of the fuel cell converters at different power levels in order to analyze the effect of the thermal stress and the calculated device lifetime.

- The lifetime investigation (with respect to bond wire and soldering fatigue) and a comparison of the three converters in a fuel cell Hybrid Electric Vehicle application are given. Moreover, it is worth to state that the lifetime of each converter is predicted based on assessing only the IGBT module.

6.3 Future work

Although many criteria has been investigated in this project, there are still possible studies that could be done. Some of these possible studies for future investigation are listed:

- Applying other methods for reliability assessments instead of the lifetime prediction from thermal point of view, but also considering other stressors as (e.g. humidity, vibration, etc.)

- Experimental validations for the thermal cycling, measurement of the junction temperature in order to validate the thermal model in the power device (IGBT) module.

- Lifetime estimation of not only the power semiconductor devices but also for other components in the converter, as the passive components (e.g. capacitors).

- Validation of the all the relevant power losses considering not only the steady state operation but also the transient state.

- More study on the influence of the design constraints on the lifetime, (e.g. same semiconductor devices, heat-sink, efficiency, etc.)

- Influence of the fuel cell/battery energy management strategy and driving cycle input on the lifetime.

- Do system level reliability analysis and study statistical variation.

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Investigation of Efficiency and Thermal Performance of the Y-source Converters for a Wide Voltage Range

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***Abstract*—The Y-source topology has a unique advantage of having high voltages gain with small shoot through duty cycles. Furthermore, having the advantage of high modulation index increase the power density and improve the performance of the converter. In this paper, a collective thermal and efficiency investigation is performed in order to improve the reliability of the converter. Losses evaluation in the semiconductor devices (switching/conduction), the capacitors (ESR), and the inductors (core/winding) are presented. Moreover, the junction temperature evaluation of the devices is considered under 25°C ambient temperature. The analysis is carried out at the following voltages gain (2, 3, and 4), and at the following winding factors (4, and 5) using PLECS toolbox. The results shows that, the power losses and the junction temperature are directly proportional with the voltage gain and the winding factor.**

I. Introduction

Y-source power converter has been used in many renewable energy applications such as; renewable generation systems [1], fuel cell applications [2], and more recently with electric vehicles [3]. Due to the importance of the thermal behaviour from the reliability point of view, a collective investigation of efficiency and thermal performance has to be done for the Y-source converter. Unreasonable temperature during the operation of the converter affects the performance, the devices lifetime, and hence, the reliability of the power electronic components in the converter. Therefore, controlling the temperature within the reasonable limits, provides: 1- higher power densities. 2- lower cost system configuration. 3- reliability improvement from lifetime point of view. 4- Increase the overall efficiency of the converter. 5- Insure safety and prevent the catastrophic design mistakes.

Practical applications requires high switching frequency with small shoot through cycles to reduce the power losses during the turn-on and turn-off transients. For a short duration, a high current passes through the switch causing high voltage stress and high junction temperature. Moreover, having higher voltages gain increase the stress in the device which needs to be designed carefully.

Thus, it is very important to consider the thermal challenges earlier in the design stage. Considering these challenges improves the performance of the converter by protecting the devices to be exposed to excessive temperatures that shorten their lifetime [4], and hence, the reliability of the converter.

This paper aims to investigate the thermal performance of the Y-source converter operating under 500 W at switching frequency of 20 kHz [5], [6], and [7]. The investigation is considered at voltages gain (2, 3, and 4), and at winding factors (4, and 5). The main sections in this paper are as the following: Section II gives the topology of the Y-source converter and its theory of operation. Section III illustrates the calculations of the efficiency and losses. Section IV presents the simulated case studies. Section V presents the simulation results and discussion, followed by the conclusion.

II. Toplogy and theory of operation

The Y-source converter is a very promising topology for higher voltage gain in a small duty ratio and in a very wide range of adjusting the voltage gain [6]. Very high modulation index can be achieved with this topology as well. The range of duty cycle in the Y-source is narrower than Z-source and the boost and higher in the modulation index. Fig.1 (a) shows the Y-source impedance network is realized a three-winding coupled inductor (N1, N2, and N3) for introducing the high boost at a small duty ratio for SW. It has an active switch SW, passive diodes (D1,D2), a capacitor C1, the windings of the coupled inductor are connected directly to SW and D1, to ensure very small leakage inductances at its winding terminals.

Fig.1 (b,c) shows the simplified circuit diagram of the ST and non shoot through NST modes of operation.

a)In the ST state, when the switch is turned on, D1 and D2 is off causing the capacitor C1 to charge the magnetizing inductor of the coupled transformer and capacitor C2 discharge to power the load.

b)In the NST state, when the switch is non-conducting, D1 start to conduct causing the input voltage to recharge the capacitor C1 and the energy from the supply and the transformer will also flow to the load and when D2 start

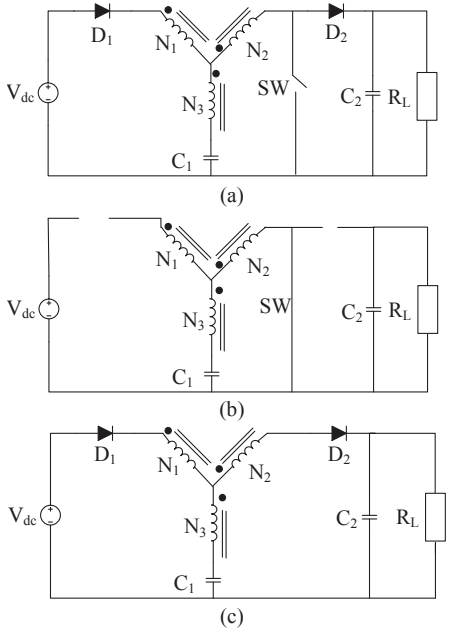

Fig. 1. illustration of a)Y-source converter, b)its equivalent "ST state", and c)its equivalent "NST state" circuits

conducting, it recharge C2 and the load to be continuously powered.

The input output voltage relation and the duty cycle is expressed in (1)

$$V_{out} = \frac{V_{in}}{(1 - KD)} \tag{1}$$

where, V_{out} is the output voltage, V_{in} is the input voltage, D is the duty cycle and K is the winding factor.

The winding factor K is calculated according to the turns ratio of the three-winding coupled inductor is expressed in (2)

$$K = \frac{N_1 + N_3}{N_3 - N_2} \tag{2}$$

where, $(N_1 : N_2 : N_3)$ is the turns ratio of the coupled inductor.

And the modulation index *M* of the Y-source is expressed in (3)

$$M = 1.15\,(1 - D) \tag{3}$$

where, D is the duty cycle required for the voltage gain and M is the modulation index.

III. Efficincy and loss calculations

In this section, further illustration for the formulas used in calculating the relevant losses and verified by the simulation results.

Having passive elements in the Y-source circuit, may have some advantages as 1) minimize the stresses according to the desired design, 2) reduces the switching and conduction losses on the devices, 3) lower shoot through duration , since they are storing energy.

A. Switching and conduction losses calculations

Switching losses occur when the device is transitioning from the blocking state to the conducting state and vice-versa. This interval is characterized by a significant voltage across its terminals and a significant current through it. The energy dissipated in each transition needs to be multiplied by the frequency to obtain the switching losses;

The switching losses P_{sw} is expressed in (4):

$$P_{sw} = (E_{on} + E_{off}) \times f_{sw} \tag{4}$$

Where, E_{on} and E_{off} are the energy losses during on and off of the switch, f_{sw} is the switching frequency.

Conduction losses occur when the device is in full conduction. The current in the device is whatever is required by the circuit and the voltage at its terminals is the voltage drop due to the device itself. These losses are in direct relationship with the duty cycle.

The average conduction losses P_{cond} is expressed in (5):

$$P_{avg.cond} = \frac{1}{T} \int_0^T \left[v_{ce}(t) \times i_{ce}(t) \right] dt \tag{5}$$

where, v_{ce} is the on state voltage, an i_{ce} is the on state current. And in (6):

$$T = \frac{1}{f_{sw}} \tag{6}$$

Time period T is inversely proportional to frequency f_{sw}.

B. Capacitor ESR losses calculations

The Equivalent Series Resistance ESR is the value of resistance which is equal to the total effect of a large set of energy loss mechanisms occurring under the operating conditions. So, the capacitors losses is expressed in (7):

$$P_{cap.loss} = I_{cap.}^2 \times ESR \tag{7}$$

where, $I_{cap.}$ is the rms current passing through the capacitor, and ESR is the equivalent series resistance measuring the effect of the losses dissipated in the capacitor.

C. Winding and core losses calculations

According to Steinmetz's equation [8], which is a physics equation used to calculate the core loss of magnetic materials due to magnetic hysteresis.

The core losses is expressed in (8):

$$P_v = k f^{\alpha} \hat{B}^{\beta} \tag{8}$$

Where, $\hat{B}$ is the peak induction of a sinusoidal excitation with frequency f, P_v is the time-average power loss per unit volume, and the material parameters (α, β, k) are material parameters.

The improved generalized Steinmetz's equation is expressed in (9):

$$P = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^a \left(\Delta B^{b-a} \right) dt \tag{9}$$

Where, ΔB is the flux density from peak to peak and in (10):

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^{\alpha} \times 2^{\beta-\alpha} d\theta} \tag{10}$$

Where, (β, α, k) are the material parameter found by curve fitting, and θ is the angle of the sinusoidal waveform simulated.

IV. Case Studies

In this section, simulations are carried out to verify the performance of the Y-source converter using the parameters listed in Table I.

TABLE I
THE USED PARAMETERS OF THE SIMULATED MODEL .

Parameters	**Values / Models**
Input voltage V_{in}	100 V - 133 V - 200 V
Output voltage V_o	400 V
Output Power P_o	500 W
Switching frequency f_s	20 kHz
Resistive load R_l	320 Ω
MOSFET *SW*	SPW47N60C3 650 V, 47 A
Diode $D_1 - D_2$	SD600N/R 600 V, 600 A
Core type V_{in}	MPP C055863A2

TABLE II
SIMULATION PARAMETERS AT THREE CASES.

Parameters	**Values**
Size of AWG	15
Winding factor K	4 5
Turns ratio $N_1 : N_2 : N_3$	80:16:48 48:16:32
DC-resistance $R_{dc-Ysource}$	0.0735 Ω 0.0441Ω
	0.0147 Ω 0.0147Ω
	0.0441 Ω 0.0294Ω

The ratings of the devices are chosen according to the voltage and current stresses across them. Where, investigating the impact of varying the voltage gain and the winding factor on the efficiency and junction temperature performances. Furthermore, measuring all the relevant losses as listed in section III. While having the same switching frequency 20 kHz, rated power 500 W, and constant ambient temperature 25 °C. Table II summarize the case studies investigated.

A. Case 1:

Simulation was carried out with voltage gain factor 2 with different value of shoot-through ratio, using winding factors 4 and 5. The rated power 500 W were applied to all the simulations.

B. Case 2:

Simulation was carried out with voltage gain factor 3 with different value of shoot-through ratio, using winding factors 4 and 5.

C. Case 3:

Simulation was carried out with voltage gain factor 4 with different value of shoot-through ratio, using winding factors 4 and 5.

V. Simulation Results and Disscusion

PLECS toolbox is used for the Y-source converter circuit . All the relevant losses results is calculated based on the aforementioned equations in the simulated model. The simulated parameters are listed in Table II. Where, the comparison is between 2 different winding factors (4, and 5), and 3 different voltage gains (2, 3, and 4), the size of the wire is 15 AWG and the values of the DC resistance is calculated according to 11:

$$R_{dc} = R_{dc/singlelayer} \times \frac{N}{L} \tag{11}$$

Where, $(R_{dc/singlelayer})$ is the dc resistance per single layer, N is the no. of turns, and L is the length of single layer.

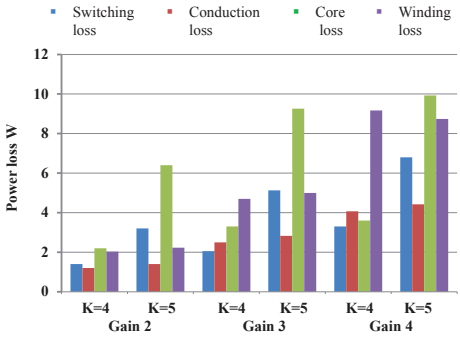

Fig. 2. Representation of the relevant losses for cases I, II, and III

TABLE III
THE SIMULATED SHOOT-THROUGH DUTY CYCLE FOR EACH CASE.

Cases	Gain	Winding factor *K*		Duty cycle *D*	
Case I	2	4	5	0.125	0.1
Case II	3	4	5	0.16674	0.133
Case III	4	4	5	0.18754	0.15

TABLE IV
THE SIMULATED SHOOT-THROUGH DUTY CYCLE FOR EACH CASE.

Cases	Winding factor *K*		Total power losses *W*		Efficiency %	
Case I - Gain 2	4	5	6.93	13.19	98.61	97.48
Case II - Gain 3	4	5	12.6	22.2	97.5	95.8
Case III - Gain 4	4	5	20.2	29.9	96.1	94.4

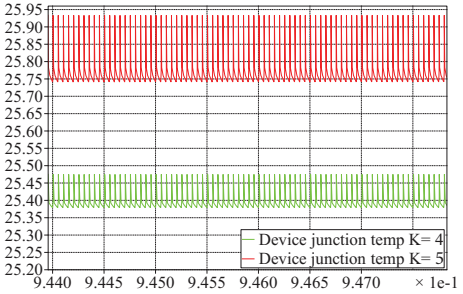

Fig. 3. Junction temperation representation at gain 2 for K= 4 and K= 5.

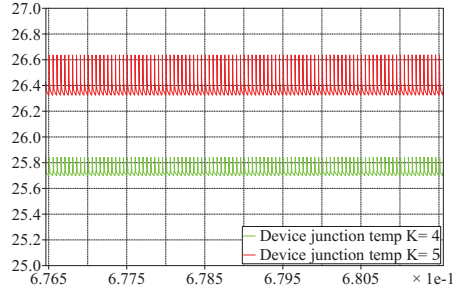

Fig. 4. Junction temperation representation at gain 3 for K= 4 and K= 5.

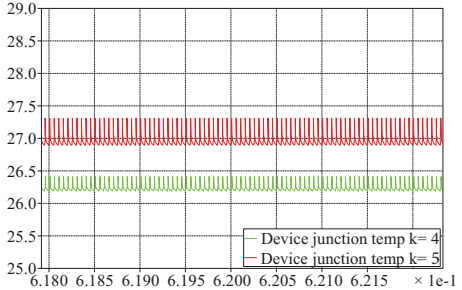

Fig. 5. Junction temperation representation at gain 4 for K= 4 and K= 5.

Fig. 2 presents the difference between the relevant losses of the devices (switching, conduction, core and winding losses) for each winding factor and voltage gain. For the capacitor ESR losses, it can be neglected, since it is very small where, the largest is 0.26 watts at gain 4 and winding factor 5. For the shoot through duty ratios for each case is listed in Table III. The simulation results indicates that the higher the voltage gain and winding factor, the higher the power losses and the junction temperature which are listed in Table IV. For the junction temperature variation in the MOSFET for different gains and winding factors in steady state, Figures 3 , 4, 5 that shows the behaviour of the junction temperature under different voltage gains and winding factors. The highest junction temperature is at voltage gain factor of 4 and winding factor of 5 as expected.

VI. Conclusion

This paper investigates the thermal performance and the efficiency of semiconductor devices and passive elements in the Y-source converter of rated power 500 W. In sake of designing a reliable converter, the thermal performance is extremely important to be considered. Measurements of the junction temperatures and relevant losses are demonstrated. The impact of different voltage gains and winding factors is performed and studied. The measurements of the junction temperature variation shows that there is no overstress on the devices during the operation, this is due to the unique advantage in the Y-source converter of having high voltage gains with very small duty ratio. The results of the relevant losses with respect to varying the voltage gains and winding factor are reasonable. It can be seen from the results that while increasing the voltage gains and the winding factors, the total power loss increase as well. The performance of the Y-source converter is very promising. Although having voltage gain factor of 4, the performance is efficient and the converter's efficiency is ranging between 94.4 % and 96 % with respect to the winding factor variation.

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Analysis of loss distribution of Conventional Boost, Z-source and Y-source Converters for wide power and voltage range

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Analysis of loss distribution of Conventional Boost, Z-source and Y-source Converters for wide power and voltage range

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Abstract— **Boost converters are needed in many applications which require the output voltage to be higher than the input voltage. Recently, boost type converters have been applied for industrial applications, and hence it has become an interesting topic of research. Many researchers proposed different impedance source converters with their unique advantages as having a high voltage gain in a small range of duty cycle ratio. However, the thermal behaviour of the semiconductor devices and passive elements in the impedance source converter is an important issue from a reliability point of view and it has not been investigated yet. Therefore, this paper presents a comparison between the conventional boost, the Z-source, and the Y-source converters based on a thermal evaluation of the semiconductors. In addition, the three topologies are also compared with respect to their efficiency. In this study the results show that the boost converter has higher efficiency than the Z-source and Y-source converter for these specific voltage gain of 2 and 4. The operational principle, mathematical derivations, simulation results and final comparisons are presented in this paper.**

Key words- boost converter; Z-source converter; Y-source converter; winding losses; core losses; gain; thermal design; reliability

I. Introduction

BOOST type converters are essentially needed for many renewable energy applications such as Photo Voltaic (PV), Wind Turbine (WT) and automotive applications (electric and hybrid vehicles) as these often have lower input voltage than the required load voltage. In conventional boost converters, the demanded voltage gain normally requires higher duty cycle (sometimes close to unity), which leads to high conduction losses, higher voltage and current stresses on the switching devices. However, the aforementioned stressor factors may critically affect the reliability and the lifetime of the power electronic components. According to a review based on condition monitoring for device reliability in power electronic systems presented in [1], semiconductor and soldering failures in device modules are sharing totally 34% of converter system failures in Fig. 1. In today's perspective toward the reliability assessment of power electronic components and systems, three main aspects should be considered as shown in Fig. 2 [2].

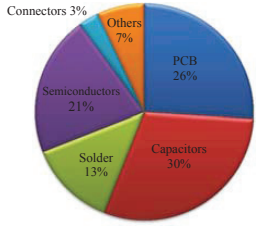


Fig. 1. Ranking and failure distrbution of power electronic components in power converters [1].

The design and verification aspect could be related to cover the aforementioned shortcomings in the conventional boost converter shown in Fig. 3. Both Z-source and Y-source as shown in Fig. 4 and Fig.5 converters were proposed by the researchers as impedance source network converters to compromise the high voltage gain with small duty cycle ratio. Due to their flexibility for a wide voltage ranges and power conversions (DC-DC, DC-AC, AC-AC, and DC-AC) [8], various types of impedance source networks were reported as a solution to overcome the limitations of the voltage source inverter VSI, current source inverter CSI and some of the conventional uni/bi - directional converters [9].

Moreover, an important advantage of the impedance net-

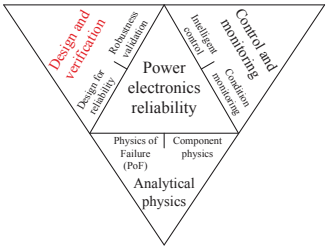


Fig. 2. Aspects in power electronics reliability assessment [2].

works is the small duty cycle ratio, which reduces the losses of the switch [10]. Therefore, many new topologies are proposed with each being claimed to have improved performances [8]. At present, a collective investigation of some of the existing boosting converters has not been initiated especially with reference to their thermal and reliability issues. Furthermore, an investigation of the Y-source converter from the point of view of thermal performance at high power ratings has not been reported as well. The junction temperature is one of the important factors that is affecting the thermal performance of the converter, and also the reliability [11].

In this paper the conventional boost, Z-source and Y-source converters are compared in terms of their efficiencies and junction temperature with respect to a wide power range, different voltage gains and assuming a constant ambient temperature. Moreover, calculations of all the relevant losses (e.g switching and conduction losses) of the power switching devices during the operation is also considered in the comparison [12].

This paper conducts a comprehensive investigation of the mapping of the losses of the power converter. Section II is focusing on the theory of operation and design of each converter. Section III describes the evaluation of the power losses and thermal performance of the three converters. Section IV describes the simulation results and discuss the results. Finally, the conclusion is given in section V.

II. Converter design and theory of operation

In this section the theory of operation of the converters and design formulas are presented.

A. Conventional boost converter

A boost converter is a step-up converter converting the voltage from low input voltage to higher voltage requiring a duty cycle (0 <D<1). Thus its simple theory of operation as well as component count wise allows it to be a competitor with other boosting converters. The basic structure of the boost converter circuit, the equivalent circuit for on state mode of operation and off state mode of operation are shown in Fig. 3. It compromise of one active switch SW, a diode D_1, an inductor L_1, and a capacitor C_1 for introducing a high voltage boost with (D>0.5). The two modes of operation are as following:

a) During the on-state: the switch is closed, the current flows through the inductor and store the energy in a magnetic field.

b) During the off-state: the switch is open, the current passed will be reduced as the voltage across the inductor is reversed and the magnetic field previously created will decrease to maintain the current flow to the load and the current through the diode will charge the capacitor giving a higher voltage.

The input/output voltage relationship is expressed in (1) as:

$$V_{out} = \frac{V_{in}}{1-D} \tag{1}$$

where V_{out} is the output voltage, V_{in} is the input voltage and D is the duty cycle needed for the required voltage gain [13].

B. Z-source converter

The Z-source converter (ZSC) is a very convenient topology in many alternative energy sources and other different applications [3, 4]. The ZSC has the capability of ideally giving an output voltage range from zero to infinity regardless of the input voltage. The Z-Source converter circuit, and its two modes of operation are shown Fig.4. It consists of two inductors (L_1, L_2) and two capacitors (C_1, C_2) connected in X shape to be coupled to the dc voltage source. The ZSC can produce a required dc output voltage regardless of the input dc source voltage. The two modes of operation are as the following:

a) In the on-state: the switch is closed and the impedance capacitors (C_1, C_2) release energy to the inductors (L_1, L_2) and then the voltage source and the load will disconnect the Z-source network due to the turn off of the diodes (D_1, D_2). The major concern is the large conduction current passing through the switch during the on state, which may decrease the converter efficiency.

b) In the off-state: the switch is opened and the input voltage will supply energy to the load through the two inductors as well as add energy to the two capacitors to compensate the energy lost during the on state.

The input/output voltage relationship is expressed in (2) as:

$$V_{out} = \frac{V_{in}}{1-2D} \tag{2}$$

where V_{out} is the output voltage, V_{in} is the input voltage and D is the duty cycle needed for the required voltage gain [3, 4].

C. Y-source converter

The Y-source converter is a promising topology for higher voltage gain in a small duty ratio and has a very wide range

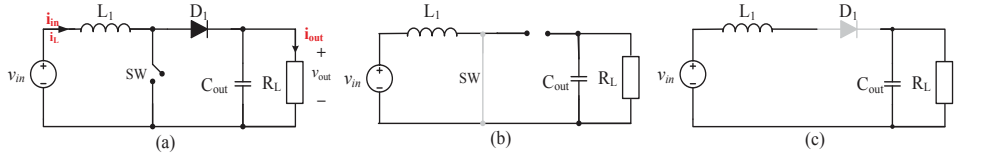


Fig. 3. a) Boost converter Circuit topology. b) Equivalent circuit for on state. c) Equivalent circuit for off state [13].

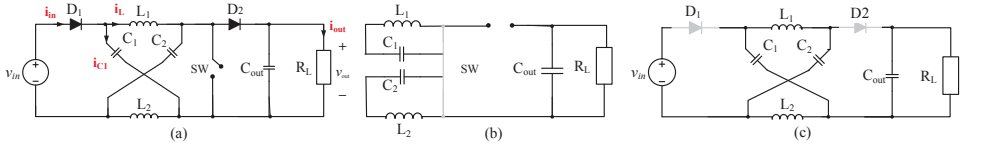


Fig. 4. a) Z-Source converter Circuit topology. b) Equivalent circuit for on state. c) Equivalent circuit for off state [3, 4].

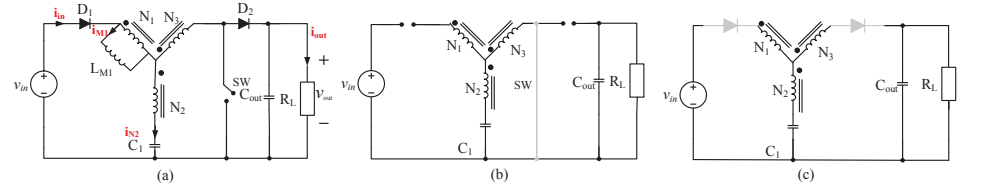


Fig. 5. a) Y-source converter Circuit topology. b) Equivalent circuit for on state. c) Equivalent circuit for off state [5–7].

of adjusting the voltage gain [5–7]. The range of duty cycle in the Y-source is narrower than the Z-source and the boost converter. Fig. 5 shows the Y-source impedance network and its two modes of operation. It is realized by a three-winding coupled inductor (N_1, N_2, and N_3) for introducing the high boost at a small duty ratio for the SW. It has an active switch SW, two diodes (D_1, D_2), a capacitor C_1, and the windings of the coupled inductor are connected directly to SW and D_1, to ensure a very small leakage inductance at its winding terminals. The two modes of operation are as the following:

a) In the on-state: the switch is closed, D_1 and D_2 are off causing the capacitor C_1 to charge the magnetizing inductor of the coupled transformer and capacitor C_2 discharge to power the load.

b) In the off-state: the switch is opened, D_1 starts to conduct causing the input voltage to recharge the capacitor C_1 and the energy from the supply and the transformer will also flow to the load. When D_2 starts conducting, it recharges C_2 and the load is to be continuously powered.

The input/output voltage relationship is expressed in (3) as:

$$V_{out} = \frac{V_{in}}{1 - KD} \tag{3}$$

where V_{out} is the output voltage, V_{in} is the input voltage, D is the duty cycle [5–7] and K is the winding factor. The winding factor K is calculated according to the turns ratio of the three-winding coupled inductor and it is expressed in (4) as:

$$K = \frac{N_1 + N_3}{N_3 - N_2} \tag{4}$$

where $(N_1 : N_2 : N_3)$ are the winding ratios of the coupled inductor.

A comparison between the inductors, the capacitors design, voltage and current ripples for the three converters is shown in Table I.

TABLE I. Component design for the Boost, Z-source and Y-source converters

Components	Boost	Z-source	Y-source
Current ripple across inductor	$\Delta I_L = 0.2 \times \frac{P_{out}}{V_{in}} = 20\% I_L$	$\Delta I_L = 20\% I_L$	$\Delta I_L = 20\% I_M$
Voltage ripple across capacitor	$\Delta V_{C_{out}} = 2\% V_{out}$	$\Delta V_C = 2\% V_{out}$	$\Delta V_{C_{out}} = 2\% V_{out}$
Inductor equation	$L = \frac{V_{in} \times D}{\Delta I_L \times f_s}$	$L = L_1 = L_2 = \frac{T_o \times V_c}{\Delta I_L}$	$L_N = A_L N^2 10^{-3}, \quad L_{lik} = \frac{0.292 \times N^{1.056} \times A_c}{L_c}$ $L = L_N + L_{lik}$
Capacitor equation	– $C_{out} = \frac{I_{out(max)} \times D}{f_s \times \Delta V_{out}}$	$C = C_1 = C_2 = \frac{T_o \times I_L}{V_c \times \%\Delta V_c}$ $C_{out} = \frac{V_{out} \times D}{R_l \times f_s \times \Delta V_{out}}$	$C_1 \geq \frac{d_{ST}}{2\%(1-D) f_s} \left(\frac{1}{1 - k D} - 1 \right) \frac{P_o}{V_o^2}$ $C_{out} = \frac{V_{out} \times D}{R_l \times f_s \times \Delta V_{out}}$

I_M: Magnetizing current, L_N: Nominal inductance, L_{lik}: leakage inductance, $T_o = DT = D/f_{sw}$

III. Evaluation of Power Losses and Thermal Performance

In this section, the formulas for calculating the relevant power losses are presented. PLECS toolbox is used for the three converter analysis. The parameters selected for each converter are compared according to the passive components counts and their voltage and current ripples are as shown in Table I. The same for the switching devices, which are designed according to each converter requirements for the voltage and current ratings for a realistic comparison.

A. Switching and conduction losses calculations

Switching losses occur when the device is transitioning from the blocking state to the conducting state and vice-versa. This interval is characterized by a significant voltage across its terminals and a significant current through it. The energy dissipated in each transition needs to be multiplied by the switching frequency to obtain the switching losses;

The switching losses P_{sw} are expressed in (5) as:

$$P_{sw} = (E_{on} + E_{off}) \times f_{sw} \tag{5}$$

where E_{on} and E_{off} are the energy losses during turn on and turn off of the switch, f_{sw} is the switching frequency.

Conduction losses occur when the device is in full conduction mode. These losses are in direct relationship with the duty cycle.

The average conduction losses P_{cond} are expressed in (6) as:

$$P_{avg.cond} = \frac{1}{T} \int_0^T [v_{ce}(t) \times i_{ce}(t)]\, dt \tag{6}$$

where v_{ce} is the on state voltage, an i_{ce} is the on state current. The time period T is as given in (7):

$$T = \frac{1}{f_{sw}} \tag{7}$$

where f_{sw} is inversely proportional to the time period T.

B. Capacitor ESR losses calculations

The Capacitor Equivalent Series Resistance (ESR) is the value of the resistance, which is equal to the total effect of a large set of energy loss mechanisms occurring under the operating conditions where it can be a parameter to measure the capacitor losses. The capacitor losses are expressed in (8) as:

$$P_{cap.loss} = I_{cap.}^2 \times ESR \tag{8}$$

where $I_{cap.}$ is the rms current passing through the capacitor, and ESR is the equivalent series resistance measuring the effect of the losses dissipated in the capacitor.

C. Winding and core losses calculations

According to the Steinmetz's equation, which is a physics based equation used to calculate the core loss of magnetic materials due to hysteresis. The core losses are expressed in (9):

$$P_v = k f^{\alpha} \hat{B}^{\beta} \tag{9}$$

where $\hat{B}$ is the peak flux density excitation with frequency f, P_v is the time-average power loss per unit volume, and(α, β, k) are the material parameters found by curve fitting.

The improved generalized Steinmetz's equation is expressed in (10):

$$P_v = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} \left(\Delta B^{\beta - \alpha} \right) dt \tag{10}$$

where ΔB is the flux density from peak to peak and in (11):

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|cos\theta|^{\alpha} \times 2^{\beta-\alpha}d\theta} \tag{11}$$

where θ is the angle of the sinusoidal waveform simulated.

The copper losses in the winding describe the energy dissipated by the resistance in the wire used in the coil. It is divided in to 2 types (DC and AC winding loss). The DC winding losses can be calculated in (12) as:

$$P_{DC} = I_{av}^2 \times R_{DC} \tag{12}$$

where *(P_{DC})* is the DC copper losses in the winding, I_{av} is the average current passing through the wire, and R_{DC} is the DC resistance of the wire.

AC copper losses can be significant for large current ripple and for higher frequency. It can be calculated through the skin effect, where the current density is an exponentially decaying function of the distance into the wire, with the characteristic length δ is known as the skin depth in (13) as:

$$\delta = \frac{7.5}{\sqrt{f_s}} \tag{13}$$

where δ is the skin depth in cm, and f_s is the switching frequency which in our design is 20 kHz.

In order to calculate the AC resistance R_{AC}, the thickness h of the wire should be known since it is a function of the dc resistance R_{DC} which can be calculated in (14):

$$R_{AC} = \frac{h}{\delta} \times R_{DC} \tag{14}$$

where h is the thickness of the wire in cm.

The AC winding losses can be calculated as given in (15) as:

$$P_{AC} = I_{AC-rms}^2 \times R_{AC} \tag{15}$$

where P_{AC} is the AC winding loss, I_{AC-rms} is AC ripple rms current passing through the wire, and R_{AC} is the AC winding resistance.

D. Magnetic core design calculations

In this section, the magnetic core design [14] is illustrated through the following steps:

1) In order to select a proper core size, the DC current I_{DC} in Ampere and the inductance L in mili Henry required with DC bias should be known to select the core from the core selector chart according to the calculated value (mH.A^2) in (16):

$$LI_{DC}^2 = \text{value} \tag{16}$$

A high flux 58337 core [14] was selected for the 3 converters in order to have fair comparison from an efficiency point of view for the voltage gain of 2.

2) Inductance, core size and permeability are now known, then calculating the number of turns by determining the minimum inductance factor A_{Lmin} by using the worst case negative tolerance (generally -8%) given in the core data sheet in (17) and (18)

$$A_{lmin} = A_l - 0.08Al \tag{17}$$

$$N = \sqrt{\frac{L \times 10^3}{A_{lmin}}} \tag{18}$$

where A_l is the inductance factor found in the core data sheet (nH/T^2), A_{lmin} is the minimum inductance factor (nH/T^2), and L is the inductance in (μH).

3) Choosing the suitable wire size according to rated power and calculated number of turns (N), is the last step before calculating the DC resistance according to the wire size with window fill assumed to be 40% in (19) as:

$$C_A = \frac{W_f \times W_A}{N} \tag{19}$$

where C_A is the wire area, W_f in the window fill, and N is the no. of turns.

4) The DC resistance can be estimated after knowing the winding factor of the core, wire gauge (AWG), and the number of turns. The DC resistance can be calculated in (20) as:

$$R_{DC} = MLT \times N \times \Omega/Length \tag{20}$$

where MLT is the mean length per turn, and $\Omega/Length$ is the resistance per meter.

Furthermore, in the voltage gain of 4 METGLAS power-lite C-core [15] is used and K_g-method is applied [16].

IV. Simulation Results and Discussion

In this section, different power loadings for the voltage gain equal to 2 and 4 are presented in order to demonstrate a fair comparison between the 3 topologies with respect to the thermal performance and the losses (switching, conduction, capacitor ESR losses, core and winding losses) for calculating the efficiency of each converter. Thermal and efficiency investigation are presented in a separate subsection. Table II summarizes the specifications and the requirements used in the simulation results.

The design specifications for each voltage gain are given separately for each topology as it can be seen from Table III, which summarize the semiconductor devices average current and voltage ratings used in the 3 converters. These ratings are based on the required voltage gain for each converter separately.

A. Junction temperature investigation of the switch under different power loading

For each semiconductor a heat sink has been designed. A maximum junction temperature of 125 °C has been used a design constraint. The estimation of the junction temperature

TABLE II. Common specifications and simulation parameters for the Boost, Z-source and Y-source converters

Common converter specifications for gain 2 and 4				
Maximum Power rating		20 kW		
Input voltage V_{in}		200 V \ 100 V *		
Output voltage V_{out}		400 V		
Switching frequency f_s		20 kHz		
Resistive load R_l		8 Ω		
Maximum junction temperature $T_{j\text{-}max.}$		125 °C		
Simulation parameters		**Boost**	**Z-source**	**Y-source**
Gain 2	Duty cycle *D*	0.5	0.25	0.167
	No. of turns	64	55	(32:32:64)
	Switch RMS current	71 A	100 A	120 A
Gain 4	Duty cycle *D*	0.75	0.375	0.25
	No. of turns	27	30	(7:7:14)
	Switch RMS current	171 A	237 A	346 A

* Input voltage for gain 4

TABLE III. Semiconductor devices selection for the three converters and their different voltage gains.

Converter	**Semiconductor devices**	**Gain 2**	**Gain 4**
Boost	**IGBT**	**(IXXX200N60C3)** 600 V and 200 A	**(MG06600WB-BN4MM)** 600 V and 600 A
	Diode (D_1)	**(IDW100E60)** 600V and 100 A	**(DB2F200N/P6S)** 600V and 200 A
Z-source	**IGBT**	**(MG06400D-BN4MM)** 600 V and 400 A	**(MG06600WB-BN4MM)** 600V and 600 A
	Diode (D_1)	**(DS1F300N6S)** 600V and 300 A	**(SD600N/R Series)** 600V and 600 A
	Diode (D_2)	**(DS1F300N6S)** 600V and 300 A	**(DS1F300N6S)** 600V and 300 A
Y-source	**IGBT**	**(MG06600WB-BN4MM)** 600V and 600 A	**(MG06600WB-BN4MM)** 600V and 600 A
	Diode (D_1)	**(VSK.9112)** 1200V and 100A	**(SKN 501/12 Semikron)** 1200V and 720 A
	Diode (D_2)	**(DS1F300N6S)** 600V and 300 A	**(DS1F300N6S)** 600V and 300 A

of the switches are done according to the thermal model and the mapped losses using the PLECS toolbox. The estimation of the junction temperatures are different for the 3 topologies, since the desired thermal resistance of the heat sink is not the exact calculated value found in the manufactured heat sinks.

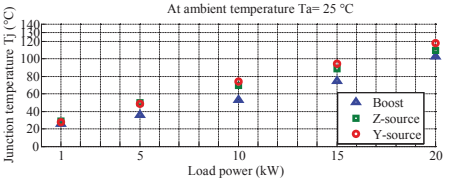


Fig. 6. Junction temperature variation of the switch at different power loading and using a voltage gain of 2.

In this case, the load power is varying from 1 to 20 kW, and a constant ambient temperature is assumed which is 25 °C. The junction temperature variation results of the compared topologies are shown in Fig. 6 for voltage gain of 2. Fig. 7 shows the junction temperature variation at different loading power for voltage gain of 4.

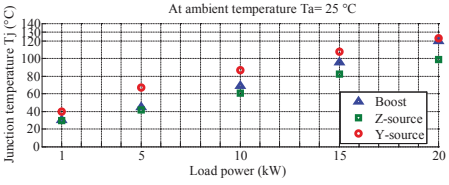


Fig. 7. Junction temperature variation of the switch at different power loading and using a voltage gain of 4.

B. Efficiency investigation under different power loading

In this subsection the efficiency is calculated according to the total power losses for each converter as listed in the beginning of section IV using the same conditions listed in

TABLE IV. Distribution of the different losses for the Boost converter at 20 kW load power and two different voltage gain.

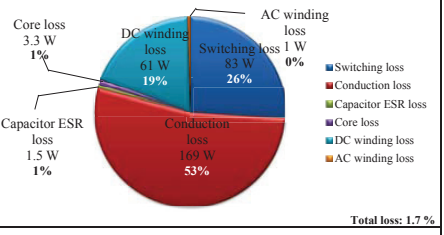
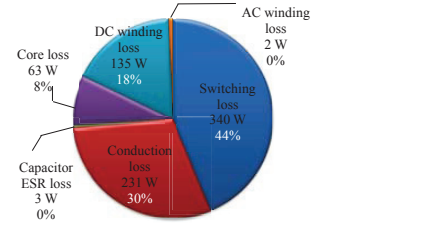
Voltage gain	Boost converter
Gain 2	
Gain 4	

TABLE V. Distribution of the different losses for the Z-source converter at 20 kW load power and two different voltage gain.

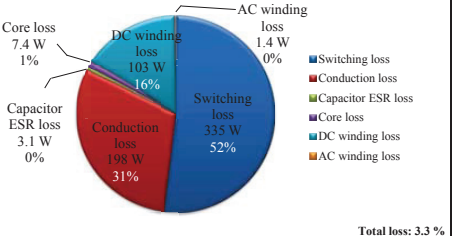
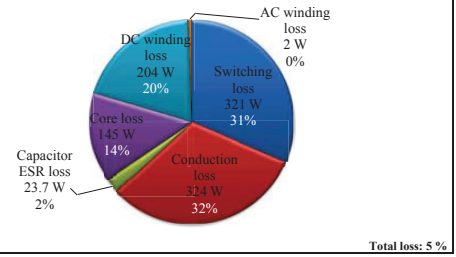
Voltage gain	Z-source converter
Gain 2	
Gain 4	

TABLE VI. Distribution of the different losses for the Y-source converter at 20 kW load power and two different voltage gain.

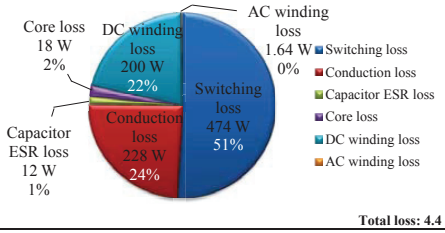
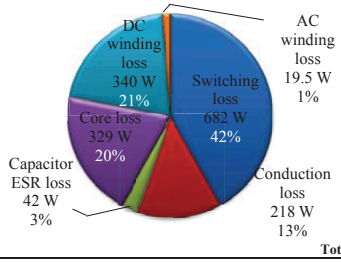
Voltage gain	Y-source converter
Gain 2	
Gain 4	

Table II. The results in Fig. 8 show that the boost converter has the highest efficiency of 98% compared with the Y-source converter of 96% and the Z-source converter of 96.7% at 20 kW loading power. The measured efficiencies from low power loading (1 kW) to higher power loading (20 kW) is also shown in 8. the same analysis is repeated for voltage gain of 4 as shown in 9.

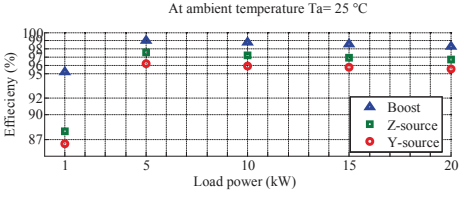


Fig. 8. The efficiency at different loading power and using a volatge gain of 2.

C. Total losses at 20 kW power loading

In this section a better understanding is given for the efficiency and loss mapping. Six pie charts are presented in Tables IV, V, and VI for the same power loading 20 kW and different voltages gain (2 and 4). The total loss listed in Table IV, V, and VI were calculated from the total power loss of each converter by measuring the total efficiency as summarized in

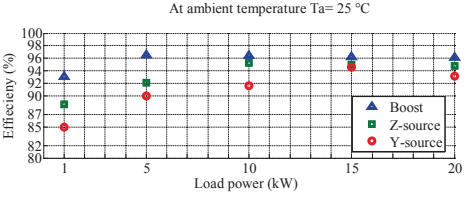


Fig. 9. The efficiency at different loading power and using a volatge gain of 4.

Table VIII. The switching and the conduction losses are the total losses generated from the semiconductor devices (switch and diodes). In Table VIII comparison of the total efficiencies using voltage gains of 2 and 4 for the compared converters at 20 kW load power.

In voltage gain 2, the magnetic losses which in the Y-source converter is sharing 34% of the total losses is the double percentage of the magnetic losses in the Z-source converter and 1.5 times the percentage in the boost converter. The capacitor losses in percentages are almost the same in the 3 converters. The switching and conduction losses are the lowest in the boost converter compared to the Z- source and Y-source converters. The switching and the conduction losses are varied based on the semiconductor devices ratings, as these devices are designed according to the required voltage gain, converter

specifications, and to withstand the maximum ratings of each operated converter.

In the voltage gain 4 case, the magnetic losses in the Y-source is sharing 42% of the total losses is more than double the percentage of the magnetic losses in the boost converter and 1.2 times the percentage in the Z-source converter.

TABLE VII. Comparison of the total efficiencies using gain 2 and gain 4 for the converters at 20 kW load.

Efficiency	Boost	Z-source	Y-source
Gain 2	98.3 %	96.7%	95.6%
Gain 4	96.1 %	95%	93.7%

V. Conclusions

In this paper a comparison between the Y-source, Z-source and the conventional boost converter has been performed with respect to their thermal behaviour and efficiency. Different loading conditions between 1 kW and 20 kW are considered during the studies of the efficiency and junction temperature of the converters for two different voltages gain (2 and 4). The junction temperature variation in voltage gain of 4 is higher than the junction temperature variation in voltage gain of 2.

Investigations on both the magnetic and electrical losses are also given. The magnetic losses which in the Y-source converter is sharing 34% and 42% of the total losses in voltage gain of 2 and 4 receptivity which is higher than in the boost and Z-source converters. In the electrical losses it can be noticed that the total electrical loss for voltage gain of 4 is lower than for voltage gain of 2 which clarify that having higher current ratings devices improve the efficiency. This paper summarizes the comparison between the type of losses at constant loading condition. The thermal performances are quite similar in the 3 converters for both voltage gains. The boost converter has better efficiencies in the two selected voltage gains, but it has also the highest decrease in the efficiency from gain 2 to gain 4 at 20 kW power loading compared with the Z-source and Y-source converters.

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A Survey on the Reliability of Power Electronics in Electro-Mobility Applications

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A Survey on the Reliability of Power Electronics in Electro-Mobility Applications

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***Abstract*—Reliability is an important issue in the field of power electronics since most of the electrical energy is today processed by power electronics. In most of the electro-mobility applications, e.g. electric and hybrid-electric vehicles, power electronic are commonly used in very harsh environment. Temperature variations, vibration and also the stresses affecting the device (which can come even from the device itself or from external sources) and may cause unreliable system. Thus, designing reliable power electronic components is important for the aim of reducing the energy losses, maintenance cost and extending the service lifetime as well. Research within power electronics is of high interest as it has an important impact in the industry of the electro-mobility applications. According to the aforementioned explanations, this paper will provide an overview of the common factors (thermal cycles, power cycles, vibrations, voltage stress and current ripple stress) affecting the reliability of power electronics in electro-mobility applications. Also, the researchers perspective is summarized from 2001 to 2015.**

I. Introduction

Power electronic components play an increasingly important role in many applications as adjustable speed drives, energy storage systems, aviation and automotive applications. The reliability of power electronics is affecting the overall system performance in these application fields. The semiconductor devices are some of the most vulnerable components in the power electronic apparatus. Therefore, any fault that occurs in the components will lead to a disorder in the system. These undesired interruptions not only affect the safety concerns, but also increases system operation cost and maintenance [1]. Nevertheless, the conditions of power electronics in mobile applications is different compared to the conditions of power electronics in photo voltaic or wind turbine systems. Thermal cycles and vibrations are one of the sever stresses in the electro-mobility applications. Also, the typical design target of lifetime in the area of automotive electronics is 15 years [26] and much less operational hours. So one of the challenges now is how to improve the reliability of the vehicles power electronic systems in the electro-mobility industry.

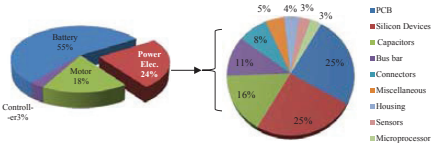

Fig. 1. Cost breakdown of power electronics in the hybrid drive system [3]

Sources of failure as vibration, humidity, power cycle, thermal cycles voltage and current stresses have an influence on the reliability of power electronics [2]. Fig. 1 shows the cost breakdown in the hybrid drive system which indicates that 24% of the cost is for power electronics. Furthermore, it is seen that 50% of the power electronics component cost is due to the silicon devices and Print-Circuit-Boards (PCBs) [3]. This paper presents a survey on different factors affecting the reliability of power electronics and some reliable solutions in this type of applications. This paper is divided in to four sections. Section II presents the source of failure in the power electronics in electro-mobility applications, section III presents the component failure in power electronics system of electro-mobility applications and section IV reliable design solutions. The conclusion is given in section V.

II. Sources of Failure in the Power Electronics for Electro-Mobility Applications

Analysis is the first step to determine which metrics should be investigated in order to evaluate and improve the reliability. Knowing the sources of failure it could be the reason to prevent the creation of failure in the initial design. Fig.2 shows the classifications of different sources of failure for which some of the power electronic components are exposed to and their reliability assessment. The different sources are discussed in the following subsections. The sources of failure which have been identified are vibration, humidity, thermal cycles, power cycles, voltage and current stresses.

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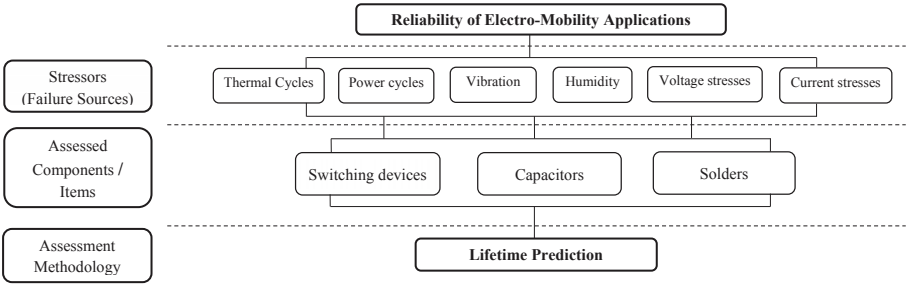


Fig. 2. Classification of reliability assessment in electro-mobility applications

A. Vibration

The combination of mechanical vibration and thermal loads are critically important in applications within the automotive, aerospace, marine, and heavy work machine industries. The reliability effect of combined thermal, thermo-mechanical, and mechanical vibration loads on solder interconnections is discussed in [4]. A single-load vibration and power cycling tests were conducted in addition to the lifetime analysis. Three different failure modes were found within all the different test cases (vibration only, constant power + vibration, power cycling + vibration and power cycling only). The cause of failure was identified in all test cases as a cracking of the solder interconnection between the component source terminal and the PCB. The lifetime trend for all of the test cases follows an inverse power function of vibration strain according to (1):

$$t_f = \left[\frac{\varepsilon - c}{a}\right]^{\frac{1}{b}} \tag{1}$$

Where ε is the board strain amplitude, a, b, and c are the fitting coefficients without direct physical meaning. Finally as a conclusion the results show that the vibration test has the most critical influence on the solder interconnections and the shortest lifetime is 2.2 minutes with strain amplitude range from 0.6×10^{-3} to 1×10^{-3} (in the test). The necessity of studying the failure mode and lifetime dependencies under combined loads can be used to reduce testing times and also to provide a reliable design in different applications, such as automotive and aviation electronics.

B. Thermal cycles

The thermal cycle stress is a response to the converter loading variations as well as the periodically commutation of power switching devices. A mechanical damage analysis of the solder joints of different types of chip resistor under thermal storage and thermal mechanical cycle condition using the EBSD (Electron Backscatter Diffraction) is discussed in [5]. The EBSD is a method that offers a better understanding of damage mechanism. EBSD is an analytic tool that can be used in combination with a scanning electron microscope [2]. After applying the thermal cycling on the joint, the damage occurred depends on directing the main grain within a solder joint with respect to the largest thermal expansion difference between joint and board. Two types of chip resistors were taken in the experiment, (CR1206 and CR0603), attached to the substrate using SnAg3.0Cu0.5 solder material. The results were compared according to the influence of constant temperature and temperature cycling. The results showed that the thermal cycling leads to much more grain structures, and induces thermo-mechanical stresses due to different coefficients of thermal expansion and material component. These correlations of grain structure to loading profile and loading duration allows for more sophisticated damage analysis.

Furthermore, another test has been performed on the solder joint reliability of ceramic chip resistors. It has been a concern for systems exposed to harsh environments such as those found in the automotive applications. In [6] the thermal cycling reliability of a 2512- chip resistor lead free solder joint configurations was investigated. In the main portion of the reliability testing, two temperature ranges (-40°C to 125°C and -40°C to 150°C) and five different solder alloys have been examined. Thermal cycling failure data has been gathered and analyzed using two parameter Weibull models to rank the relative material performances and a set of thermally cycled sample for microscopy studies as cracks propagation and change in the micro-structure of solders. A 63Sn- 37Pb joint dramatically outperformed the lead free Sn- Ag-Cu alloy joints for the more extreme (-40°C to 150°C) testing. Such results further underscore the need to be cautious when proposing lead-free solder substitutions for SMT configurations in harsh environments. Failure analysis has shown that the solder joint cracking and creep-fatigue damage propagates as expected for chip resistors.

C. Power cycles

Power Cycling is a common procedure to investigate the reliability of power electronic devices, especially power modules. There are two types of power cycle on test: 1. The

junction temperature power cycle; (where Tj is the temperature in the junction region of a semiconductor chip). The higher the maximum junction temperature, the higher is the stress to the device which results in a reduced number of cycles. 2. The case temperature power cycle, where the thermal cycling raises and lowers the case temperature (T_c) at relatively long intervals of time (minutes). The power cycling capability of power semiconductor modules is dependent on absolute junction temperature (T_j), the temperature swing (ΔT_j) and the duration (T_{cyc}, T_{on}) of the power cycle. The reliability of the module regarding the thermal stress conditions over the lifetime are used in HEV among power cycling and thermal cycling tests [23]. In a combination of the electrical properties and thermal behavior of a power module, a loss profile can be calculated and these losses models can generate the temperature profiles on the IGBTs and diodes. Furthermore, in order to calculate a temperature profile from the losses, a thermal model of the power module including the cooling system must be included. An automatic algorithm is implemented to extract temperature swings because of different thermal resistance values in the system. The power cycling capability is influenced by the junction temperature, the duration of loss generation, and the current. A test cycle was performed with the following paramteres; $\Delta T_{test} = 100$ K, $\mathrm{Tj}_{max} = 150$ °C, $T_{on} = 2$ s at 800 A. The calculation results is approx. 4000 power cycles for the IGBT and the diode.

Another test has been performed for the IGBT module on a passive thermal cycling and power cycling [24]. In the thermal cycling, the IGBT module is mounted by a layer of thermal grease into a combined heater and heat sink system and undergoes passive temperature swings. The temperature excursion is expressed in terms of the temperature at the bottom of the base plate. Typically, ΔT_c is set within the range of 60 K to 100 K. The failure criterion in this test, is increase of the thermal resistance of 20%. In the power cycling test, the IGBT module is mounted on a heat sink. The dies are actively heated by a current causing power loss in the dies. The typical on-time is from seconds to minutes depending on the maximum junction temperature and swing excursion. Due to the direct heating of the dies power cycling allows a very fast ramp up of the junction temperature Tj and the case temperature Tc. The End Of Life (EOL) failure mechanisms in the power cycling and thermal cycling are different. The first leads to a forward voltage drop increase whereas the second leads to a thermal resistance increase. The results shows, the temperature swing in the solder corners is lower than that at the case below the chip positions. However, cracks in the solder start at the corners. The experimental data from the test suggest that the substrate solder at low temperature swings behaves as expected from a power law extrapolation of the passive thermal cycling data gathered at higher temperature excursions. This allows for the determination of the temperature swing of any part in the module during the power cycling.

III. Component Failure in Power Electronic Systems of Electro-Mobility Applications

One of the most important challenges in the vehicles manufacture is to consider the component failure rate estimation. Therefore, Fig. 3 shows an overview during the past 15 years on the components failure and their reliability assessments methods which had been proposed by different researchers in the literature. The switching devices are one of the most critical components that the researchers focused on in the electro-mobility applications.

A. Switching devices

Selecting a reliable switching devices for automotive system should serve the lifetime targets. Also the necessity of the ageing behaviour of the components and understanding the effect of the steady state and varying failure rates have influences on the system performance. In [8] the importance of the components physics of failure approach for accurate failure rate estimates that have to influence the target robust system architecture. Usually the component failure rate is estimated in accordance to (2):

$$\lambda_{ref}(\text{random}) \leq \frac{X^2(cl*(f+2))}{N*t_{test}*A_f} \tag{2}$$

where, X^2 is the Chi-square distribution, cl is the confidence level, f is the number of failures in test, N is the number of tested parts, t_{test} is the test (stress) time, and A_f is the stress parameter. Based on the principles of the dependence between system reliability and component reliability, the failure rate can be estimated based on simple failure rate calculations by (3):

$$\lambda_{actual}(\text{life phase,t}) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} \tag{3}$$

where, β is the Weibull shape parameter, and η is the Weibull scale parameter. Few cases were presented, and the simulations were linked to a real case in an automotive power system with insulated gate bipolar transistor (IGBT) module. Also as the number of switching devices into a vehicle increases, it is necessary to pay attention to pattern changes and also to the associated increasing robustness requirements.

B. Capacitors

Capacitors are widely used in many automotive electronic systems and their quality, stability and reliability have been analysed by automotive producers [9]. Since electric vehicles are in widespread use, the electronic systems and components that have enabled the realization of such a wide variety of electric vehicles have all experienced a major evolution, including the DC link power capacitor. Capacitors are also exposed to harsh environments in this application. The purpose of capacitors in electric vehicles is to reduce ripple currents of power source, and to smoothen out DC bus voltage variations. One major advantage is the ability of film capacitors to overcome internal defects. As a result, there is no complete failure and no short circuit, only a minimum capacitance decrease

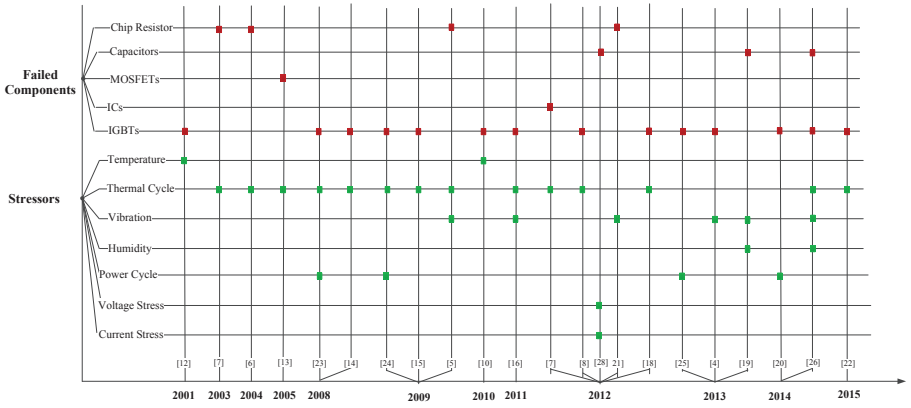


Fig. 3. Overview of sources of failure and failure components of power electronics

which can be useful as a measure of ageing. It offers the space savings and no expansion problems across temperature variation range (-55°C to +125°C). DC link capacitor development has to match the evolution in power semiconductor technology not only electrically, but also mechanically. Finally, the tantalum capacitors also offer enhanced reliability (failure rate 0.5%/1000 hours) and a higher category voltage at 125 °C (78% of rated voltage) than standard devices (typically only 66% of rated voltage).

C. Solders in power electronic module

The Power Electronic Modules (PEMs) are widely used in aerospace and automotive applications with the essentiality of high reliability. Solder fatigue is one of failure mechanisms in PEMs and thus a reliability assessment method for this failure mechanism is presented [10]. Insulated Gate Bipolar Transistor (IGBT) is one of the components which often works under heavy work load conditions and in harsh environment. Thus, their required reliability standard is often high. In service, PEMs often generate a large amount of heat, and the induced high temperature and temperature swings causes thermal stresses in the modules. As a result, cracks are initiated and propagated in the solder layer; eventually this will cause a rise in semiconductor junction temperature and lead to the failure of the module. Fig. 4 illustrates the steps of implementing the lifetime estimation of the module. The reliability assessment method of the whole system can be divided into two sections: 1) Compact electro-thermal model, 2) Compact thermal-mechanical model. In the temperature profile, it consists of different temperature change amplitudes and mean values. A rain flow counting algorithm can be applied to extract the numbers of cycles with certain temperature ranges so accumulated damage is predicted.

IV. Lifetime Prediction Methods

Reliability calculation is one of the most critical drivers, where emerging technologies requirements is very high in order to be designed into these types of applications. Thus, this field of reliability must be approached at the most fundamental level when evaluating and predicting the products lifetime. Some of the selected lifetime prediction methods are classified in details and Table I provides an overview on how to be applied for various power electronics components.

Table II shows a summary of some of the based approaches used by prior-art in lifetime prediction of some power electronic components.

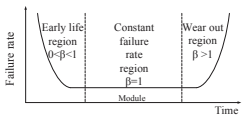
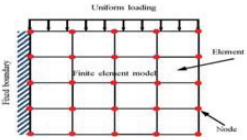
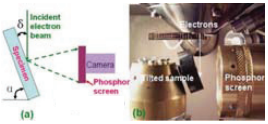
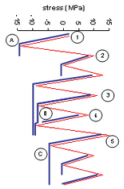
A. Capacitors life time model

1) Voltage stress: Capacitors are one of the most vulnerable components in terms of failure level and time as analyzed in [26]. Therefore, knowing how to predict the life time of the capacitors would reduce the cost and insure safety. Lifetime prediction of capacitors is mainly based on empirical models as physical-based models are still not achieved. The most widely used empirical model for capacitors is shown in (4), which describes the influence of temperature and voltage stress.

$$L = L_{\circ} \times \left(\frac{V}{V_{\circ}}\right)^{-n} \times exp[\left(\frac{E_a}{K_B}\right)\left(\frac{1}{T} - \frac{1}{T_{\circ}}\right)] \quad (4)$$

Where L and $L_{\circ}$ are the lifetime under the use condition and testing condition. V and $V_{\circ}$, are the voltage at use and test conditions. T and $T_{\circ}$ are temperature in Kelvin at use and test conditions. E_a is the activation energy, K_B is Boltzmanns constant $(8.62105eV/K)$, and n is the voltage stress exponent. Therefore, the values of E_a and n are the key parameters to be determined in the above model.

TABLE I. Different methods of lifetime prediction and assessment

Methods	Definitions	Math. Equations	Models
Weibull distribution & Failure rate	Frequently used to model fatigue failure.	$F(t) = 1 - \exp[-(\frac{t}{\eta})^{\beta}]$ F: Probability of failure t: Test statistics (e.g. no. of cycle) η: Characteristics life β: Shape parameter	
Finite element	A numerical method for solving a system of governing equations over a domain of a continuous physical system in to simple geometric shape.	$\{U\} = [K]^{-1}\{F\}$ U: Behavior (e.g. temperature, velocity, …) K: Property (e.g. conductivity, viscosity, …) F: Action (e.g. heat source, force, …)	
Electron backscatter diffraction	A beam of electrons is directed at a point of interest on a tilted crystalline sample by 70°.	$n\lambda = 2d\sin\theta$ n: positive integer λ: is the wavelength of incident wave	
Rain flow counting	A method for counting fatigue cycles from a time history and these fatigue cycles are stress-reversals.	The stress history should be reduced to peaks and valleys by software. (e.g. using Matlab)	

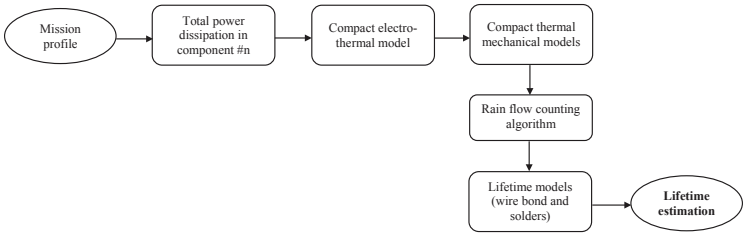


Fig. 4. Power electronic module lifetime estimation based on mission profile and rain flow counting algorithm [10]

2) Current ripple stress: DC-link (dc) capacitors are bulky, heavy, and expensive. Nerveless of their importance to attenuate ripple current, reduce emission of electromagnetic interference, and suppress voltage spikes caused by leakage inductance and switching operations in the electric vehicles (EV) inverter systems [28].

The ripple current is one of the main considerations in sizing and selecting dc-link capacitors. In EV inverter systems, the capacitor ripple current consists of various frequency components that correspond to different PWM strategies. Furthermore, the electro-thermal coupling dynamics must be evaluated in order to estimate the true core temperature of the

TABLE II. A summary of lifetime prediction based approaches

Assessed Component	Stressor	Based Approach	Ref
Chip Resistors (solders)	Thermal cycling	Weibull model	[7][6][1]
	Thermal cycling	Electron Backscatter Diffraction (EBSD)	[5]
	Vibration		
IGBT	Thermal cycling	Electron Backscatter Diffraction (EBSD)	[16]
	Vibration		
	Temperature	Finite Element Method (FEM)	[12][10]
	Thermal cycling	Finite Element Method (FEM)	[14][15][20] [22]
	Thermal cycling	Weibull model	[8]
	Vibration	Finite Element Method (FEM)	[4]
	Power cycling	Finite Element Method (FEM)	[23][24]
	Thermal cycling	Rain flow counting algorithm	[25]
Capacitors	Thermal cycling	Failure rate model	[19]
	Voltage stresses	Empirical model	[26]
	Current ripple stresses	Life time model	[28]

dc-link capacitors, which is critical to predict the capacitor lifetime. The maximum current stress I_{cap} on a dc link capacitor can be expressed by (5) over a wide variety of operating conditions for a specific motor, modulation method, and battery:

$$I_{cap} = I_N \sqrt{\frac{M}{32\pi}[4\sqrt{3}(4cos2\phi + 6) - 9\pi \quad M \quad (cos2\phi + 1)]} \tag{5}$$

Where *M* is the modulation index, I_N is the output phase current amplitude, and ϕ is the phase delay of the inverter output current with respect to the voltage fundamental.

The capacitor lifetime also is influenced by the capacitor core temperature and the ripple current which can be expressed by (6).

$$L_e = L_b \quad 2^{\frac{T_{jc}-T_a}{10}} \quad K^{\left[\frac{I}{I_\circ}^2\right]\left[\frac{\Delta T_{jc}}{10}\right]} \tag{6}$$

where L_b is the capacitor lifetime under its maximum temperature and it is commonly given by the manufacturer data sheets. $I_\circ$ denotes the allowable maximum current ripple at a given frequency, which is also given in data sheets, and *I* denotes the actual current ripple value. *K* is a constant, which is typically assigned to a value of 2. T_{jc} is the junction to case temperature, T_a is the ambient temperature.

B. IGBT module life time model

There are three dominant wear-out failure mechanisms for the IGBT modules due to thermal cycle stress: 1) baseplate solder joints cracking; 2) chip solder joint cracking; and 3) the wire bonds lift off. Fig. 5. shows a detailed structure of an IGBT module classified into different material in the module with their thermal expansion and it leads to stress formation in the packaging and continuous degradation during each cycle until the material fails.

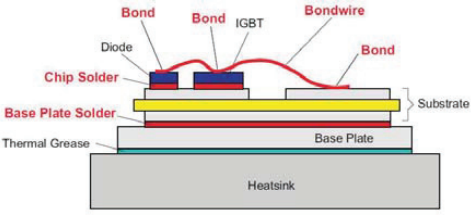


Fig. 5. A detailed structure of an IGBT module.

The model shown in (7) derives the number of cycles to failure under thermal cycling.

$$N = k(\triangle T - \triangle T_\circ)^{-m} \tag{7}$$

Where *k* and m are empirically determined constants and *N* is the number of cycles to failure. $\triangle T$ is the thermal cycling range and $\triangle T_\circ$ s the portion of $\triangle T$ that in the elastic strain range. If $\triangle T_\circ$ is negligible compared with $\triangle T$, it can be concluded from the above equation which then becomes the Coffin-Manson model which previously discussed in [27].

V. Conclusions

In this paper a review of the reliability of power electronic in electro-mobility applications has been carried out in order to provide a picture of the current status in this particular research field. The goal with reliability engineering is to prevent the creation of failures and extend the service life

time as well. Reliability is the most important performance in the power electronics index. As it has a great influence in the industry of most of the application as (power transmissions, power distributions, aerospace and automotive applications). Different sources of failure, failed components and methods of the lifetime reliability assessments have been presented. Aiming for introducing new reliability assessments and validation methods in the area of automotive electronics.

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Thermal Performance and Efficiency Investigation of Conventional Boost, Z-source and Y-source Converters

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Thermal Performance and Efficiency Investigation of Conventional Boost, Z-source and Y-source Converters

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***Abstract*— Boost converters are needed in many applications that require the output voltage to be higher than the input voltage. Recently, boost type converters have been attracted by the industrial applications, and hence it has become an extremely hot topic of research. Recently, many researchers proposed the impedance source converters with their unique advantages as having a high voltage gain in a small range of duty cycle ratio. However, the thermal behaviour of the semiconductor devices and passive elements in the impedance source converter is an important issue from a reliability point of view and has not been investigated yet. Therefore this paper presents a comparison between the conventional boost, the Z-source, and the Y-source converters based on the thermal evaluation of semiconductors. In addition, the three topologies are also compared with respect to their efficiency. The operational principle, mathematical derivations, simulation results and finally conclusion comparisons are presented in this paper.**

Key words- boost converter; Z-source converter; Y-source converter; winding losses; core losses; gain; thermal; reliability

I. Introduction

Boost type converters are essentially needed for many renewable energy applications such as Photo Voltaic (PV), Wind Turbine (WT), automotive applications (electric and hybrid vehicles) as these often have lower input voltage than the required load voltage. In conventional boost converters, the demanded voltage gain normally requires higher duty cycle (sometimes close to unity) which leads to high conduction losses, higher voltage and current stresses on the switching devices. However, the aforementioned stressor factors may critically affect the reliability and the lifetime of the power electronic components. According to a review based on condition monitoring for device reliability in power electronic systems presented in [1], semiconductors and soldering failures in device modules are sharing totals 34% of converter system failures. In today's perspective toward the reliability assessment of power electronic components and systems, three main aspects should be considered as shown in Fig. 1 [2].

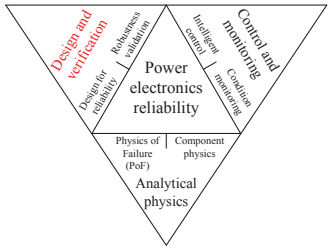

Fig. 1. Aspects of power electronics reliabilty assessment [2].

The design and verification aspect could be related to cover the aforementioned shortcomings in the conventional boost converter shown in Fig. 2. Both Z-source and Y-source as shown in Fig. 3 and Fig. 4 converters were proposed by the researchers as impedance source network converters to compromise the high voltage gain with small duty cycle ratio. Due to their flexibility for a wide voltage ranges and power conversions (DC-DC, DC-AC, AC-AC, and DC-AC) [3], various types of impedance source networks were reported as a solution to overcome the limitations of the voltage source inverter VSI, current source inverter CSI and some of the conventional uni/bi - directional converters [4].

Moreover, an important advantage of the impedance networks is the small duty cycle ratio, which reduces the voltage stress experienced by the component, and reduces the losses of the switch as well [5]. Therefore, many new topologies are proposed with each being claimed to have improved performances [3]. At present, a collective investigation of some of the existing boosting converters has not been initiated especially with reference to their thermal and reliability issues. Furthermore, an investigation on the Y-source converters from the point of view of thermal performance at high power ratings has not been reported as well. The junction temperature is

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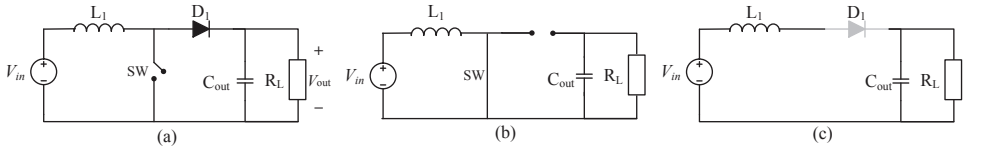

Fig. 2. a) Conventional boost converter equivalent circuit. b) Equivalent circuit for on state. c) equivalent circuit for off state.

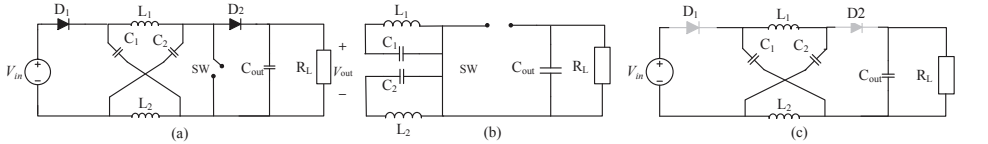

Fig. 3. a) Z-Source converter equivalent circuit. b) Equivalent circuit for on state. c) Equivalent circuit for off state.

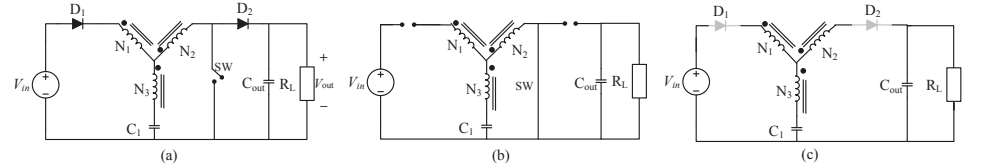

Fig. 4. a) Y-source converter equivalent circuit. b) Equivalent circuit for on state. c) Equivalent circuit for off state.

one of the important factors that is affecting the thermal performance of the converter, and also the reliability [6].

In this paper the conventional boost, Z-source and Y-source converters are compared from the point of view of their efficiencies and junction temperature with respect to a wide power range and in a constant ambient temperature. Moreover, calculations all the relevant losses (e.g switching and conduction losses) of the power switching devices during the operation is considered in the comparison.

This paper conducts a comprehensive investigation of the research topic of power converter. Section II is focusing on the theory of operation and design of each converter. Section III describes the evaluation of the power losses and thermal performance of the three converters. Section IV describes the simulation results and gives also discussion. Finally, the conclusion is given in section V.

II. Converter design and theory of operation

In this section the theory of operation and design formulas are presented.

A. Conventional boost converter

A boost converter is a step up converter from low input voltage to higher voltage requiring a duty cycle (0 <D<1). Thus its simple theory of operation as well as component count wise allows it to be a competitor with other boosting converters. The basic structure of the boost converter circuit, equivalent circuit for on state mode of operation and off state mode of operation are shown in Fig. 2. It compromise one active switch SW, a diode D_1, an inductor L_1, and a capacitor C_1 for introducing a high voltage boost with (D>0.5). The two modes of operation are as following:

a) During the on state: the switch is closed, the current flows through the inductor and store the energy by the generating magnetic field.

b) During the off state: the switch is open, the current passed will be reduced as the voltage across the inductor is reversed and the magnetic field previously created will decrease to maintain the current flow to the load and the diode will charge the capacitor with higher voltage.

The input/output voltage relationship and the duty cycle is expressed in (1):

$$V_{out} = \frac{V_{in}}{1 - D} \tag{1}$$

where V_{out} is the output voltage, V_{in} is the input voltage and D is the duty cycle needed for the required voltage gain.

B. Z-source converter

The Z-source converter (ZSC) is very convenient topology in many alternative energy sources and other different

applications [7, 8]. The ZSC has the capability of ideally giving an output voltage range from zero to infinity regardless of the input voltage. The Z-Source converter circuit, and its two modes of operation are shown Fig.3. It consists of two inductors (L_1, L_2) and two capacitors (C_1, C_2) connected in X shape to be coupled to the dc voltage source. The ZSC can produce a required dc output voltage regardless the input dc source voltage. The two modes of operation are as the following:

a) In the on state: the switch is closed and the impedance capacitors (C_1, C_2) release energy to the inductors (L_1, L_2) and then the voltage source and the load will disconnect the Z- source network due to the turn off of the diodes (D_1, D_2). The major concern is the large conduction current passing through the switch during the on state, which may decrease the converter efficiency.

b) In the off state: the switch is opened and the input voltage will supply energy to the load through the two inductors as well as add energy to the two capacitors to compensate the energy lost during on state.

The input/output voltage relationship and the duty cycle is expressed in (2):

$$V_{out} = \frac{V_{in}}{1 - 2D} \tag{2}$$

where V_{out} is the output voltage, V_{in} is the input voltage and D is the duty cycle needed for the required voltage gain.

C. Y-source converter

The Y-source converter is a very promising topology for higher voltage gain in a small duty ratio and in a very wide range of adjusting the voltage gain [9–11]. The range of duty cycle in the Y-source is narrower than the Z-source and the boost converter. Fig. 4 shows the Y-source impedance network and its two modes of operation. It realized by a three-winding coupled inductor (N_1, N_2, and N_3) for introducing the high boost at a small duty ratio for SW. It has an active switch SW, two diodes (D_1, D_2), a capacitor C_1, and the windings of the coupled inductor are connected directly to SW and D_1, to ensure a very small leakage inductance at its winding terminals. The two modes of operation are as following:

a) In the on state: the switch is closed, D_1 and D_2 are off causing the capacitor C_1 to charge the magnetizing inductor of the coupled transformer and capacitor C_2 discharge to power the load.

b) In the off state: the switch is opened, D_1 start to conduct causing the input voltage to recharge the capacitor C_1 and the energy from the supply and the transformer will also flow to the load. When D_2 starts conducting, it recharges C_2 and the load is to be continuously powered.

The input/output voltage relationship and the duty cycle is expressed in (3):

$$V_{out} = \frac{V_{in}}{1 - KD} \tag{3}$$

where V_{out} is the output voltage, V_{in} is the input voltage, D is the duty cycle and K is the winding factor. The winding factor K is calculated according to the turns ratio of the three-winding coupled inductor and expressed in (4):

$$K = \frac{N_1 + N_3}{N_3 - N_2} \tag{4}$$

where $(N_1 : N_2 : N_3)$ are the winding ratios of the coupled inductor.

A comparison between the inductors, the capacitors design, voltage and current ripples for the three converters is shown in Table I.

III. Evaluation of power losses and thermal performance

In this section, formulas for calculating the relevant power losses are presented. PLECS toolbox is used for the three converter analysis. The parameters selected for each converter are compared according to the passive components counts and their voltage and current ripple are as shown in Table I. The same for the switching devices, which are designed according to each converter requirements for the voltage and current ratings for a realistic comparison.

A. Switching and conduction losses calculations

Switching losses occur when the device is transitioning from the blocking state to the conducting state and vice-versa. This interval is characterized by a significant voltage across its terminals and a significant current through it. The energy dissipated in each transition needs to be multiplied by the switching frequency to obtain the switching losses;

The switching losses P_{sw} are expressed in (5) as:

$$P_{sw} = (E_{on} + E_{off}) \times f_{sw} \tag{5}$$

where E_{on} and E_{off} are the energy losses during turn on and turn off of the switch, f_{sw} is the switching frequency.

Conduction losses occur when the device is in full conduction mode. These losses are in direct relationship with the duty cycle.

The average conduction losses P_{cond} are expressed in (6) as:

$$P_{avg.cond} = \frac{1}{T} \int_0^T [v_{ce}(t) \times i_{ce}(t)]\, dt \tag{6}$$

where v_{ce} is the on state voltage, an i_{ce} is the on state current. The time period T is as given in (7):

$$T = \frac{1}{f_{sw}} \tag{7}$$

where f_{sw} is the inversely proportional to time period T.

TABLE I. Components design for the Boost, Z-source and Y-source converters

Components	Boost	Z-source	Y-source
Current ripple across inductor	$\Delta I_l = 0.2 \times \frac{P_{out}}{V_{in}} = 20\% I_L$	$\Delta I_l = 20\% I_L$	$\Delta I_l = 20\% I_L$
Voltage ripple across capacitor	$\Delta V_{C_{out}} = 2\% V_{out}$	$\Delta V_C = 2\% V_{out}$	$\Delta V_{C_{out}} = 2\% V_{out}$
Inductor equation	$L = \frac{V_{in} \times D}{\Delta I_L \times f_s}$	$L = L_1 = L_2 = \frac{T_o \times V_c}{\Delta I_L}$ Where, $T_o = DT$	$L^* = A_L N^2 10^{-3}, \quad L_{lik} = \frac{0.292 \times N^{1.056} \times A_c}{L_c}$ $L = L^* + L_{lik}$
Capacitor equation	– $C_{out} = \frac{I_{out(max)} \times D}{f_s \times \Delta V_{out}}$	$C = C_1 = C_2 = \frac{T_o \times I_L}{V_c \times \%\Delta V_c}$ $C_{out} = \frac{V_{out} \times D}{R_l \times f_s \times \Delta V_{out}}$	$C_1 \geq \frac{d_{ST}}{2\%(1-D)f_s}\left(\frac{1}{1-kD}-1\right)\frac{P_o}{V_o^2}$ $C_{out} = \frac{V_{out} \times D}{R_l \times f_s \times \Delta V_{out}}$

B. Capacitor ESR losses calculations

The Equivalent Series Resistance ESR is the value of the resistance, which is equal to the total effect of a large set of energy loss mechanisms occurring under the operating conditions. So the capacitors losses are expressed in (8) as:

$$P_{cap.loss} = I_{cap.}^2 \times ESR \tag{8}$$

where $I_{cap.}$ is the rms current passing through the capacitor, and ESR is the equivalent series resistance measuring the effect of the losses dissipated in the capacitor.

C. Winding and core losses calculations

According to the Steinmetz's equation, which is a physics equation used to calculate the core loss of magnetic materials due to magnetic hysteresis, the core losses is expressed in (9):

$$P_v = k f^{\alpha} \hat{B}^{\beta} \tag{9}$$

where $\hat{B}$ is the peak flux density excitation with frequency f, P_v is the time-average power loss per unit volume, and the material parameters (α, β, k) are material parameters.

The copper losses in the winding describe the energy dissipated by resistance in the wire used to wind a coil. It is divided in to 2 types (DC and AC winding loss). The DC winding losses, can be calculated in (10) as:

$$P_{DC} = I_{av}^2 \times R_{DC} \tag{10}$$

Where, (P_{DC}) is the DC copper losses in the winding, I_{av} is the average current passing through the wire, and R_{DC} is the DC resistance of the wire.

AC copper losses can be significant for large current ripple and for high frequency. It can be calculated through the skin effect, where the current density is an exponentially decaying function of the distance into the wire, with characteristic length δ is known as the skin depth in (11):

$$\delta = \frac{7.5}{\sqrt{f_s}} \tag{11}$$

where δ is the skin depth in cm, and f_s is the switching frequency which in our design is 20 kHz.

In order to calculate the AC resistance R_{AC}, the thickness h of the wire should be known since it is a function of the DC resistance R_{DC} which can be calculated in (12):

$$R_{AC} = \frac{h}{\delta} \times R_{DC} \tag{12}$$

where h is the thickness of the wire in cm.

The AC winding losses can be calculated as given in (13) as:

$$P_{AC} = I_{AC-rms}^2 \times R_{AC} \tag{13}$$

Where, P_{AC} is the AC winding loss, I_{AC-rms} is AC ripple rms current passing through the wire, and R_{AC} is the AC winding resistance.

D. Magnetic core design calculations

In this section, the magnetic core design [12] is illustrated through the following steps:

1) In order to select a proper core size, the DC current and the inductance required with DC bias should be known to select the core from the core selector chart according to the calculated value in (14):

$$LI_{DC}^2 \Rightarrow (mH.A^2) \tag{14}$$

A high flux 58337 core [12], were selected for the 3 converter in order to have fair comparison from an efficiency point of view.

2) Inductance, core size and permeability are now known, then calculating the no. of turns by determine the minimum

TABLE II. Common specifications and simulation parameters for the Boost, Z-source and Y-source converters

Common specifications			
Maximum Power rating	20 kW		
Voltage gain	2		
Input voltage V_{in}	200 V		
Output voltage V_{out}	400 V		
Switching frequency f_s	20 kHz		
Resistive load R_l	8 Ω		
Maximum junction temperature $T_{j\text{-}max.}$	125 °C		
Simulation parameters	**Boost**	**Z-source**	**Y-source**
Duty cycle	0.5	0.25	0.167
No. of turns	64	55	(32:32:64)
RMS current per device	71 A	100 A	120 A
MAX voltage per device	400 V	400 V	400 V

inductance factor A_{Lmin} by using the worst case negative tolerance (generally -8%) given in the core data sheet in (15) and 16

$$A_{lmin} = A_l - 0.08Al \tag{15}$$

$$N = \sqrt{\frac{L \times 10^3}{A_{lmin}}} \tag{16}$$

where A_{lmin} is the minimum inductance factor (nH/T^2), and L is the inductance in (μH).

3) The DC resistance can be estimated after knowing the winding factor of the core, wire gauge (AWG), and the no. of turns. The DC resistance can be calculated in (17) as:

$$R_{DC} = MLT \times N \times \Omega/Length \tag{17}$$

Where, MLT is the mean length per turn, and $\Omega/Length$ is the resistance per meter.

IV. Results and Discussion

In this section, different power loading for the voltage gain equal to 2 are presented in order to demonstrate fair comparison between the 3 topologies with respect to the thermal performance and the losses (switching, conduction, capacitor ESR losses, core and winding losses) for calculating the efficiency of each converter.

Thermal and efficiency investigation are presented in a separate subsection. Table II summarizes the specifications and the requirements used in the simulation results.

A. Junction temperature investigation of the switch under different power loading

Based on designing a proper heat sink, where it is assumed 125 °C is the maximum allowable junction temperature for the device and also the amount of heat losses generated from the devices in each topology. The estimation of the junction temperature of the switches are done according to the thermal model and the mapped losses using PLECS toolbox. The estimation of the junction temperatures are different for the 3 topologies, since the desired thermal resistance of the heat sink is not the exact value found in the manufactured heat sinks.

In this case, the power loading is varying from 5 to 20 kW, and constant ambient temperature is assumed which is 25 °C. The results of the compared topologies are shown in Fig. 5.

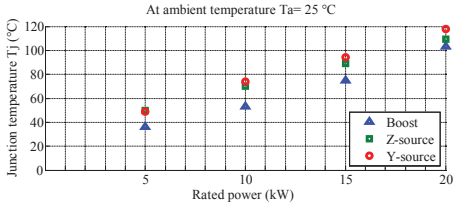

Fig. 5. Junction temperature variation at different power loading of the switch.

B. Efficiency investigation under different power loading

In this subsection the efficiency is calculated according to the total power losses for each converter as listed in the beginning of section IV using the same conditions listed in Table 2. The results in Fig. 6 shows that the boost converter has the highest efficiency of 98% compared with the Y-source converter 96% and the Z-source converter 96.7% at 20 kW loading power.

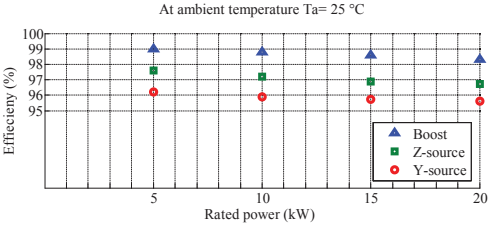

Fig. 6. The efficiency at different loading power.

Also to give a better understanding of the distribution of each type of losses, three pie charts are presented in Fig. 7, Fig. 8, and Fig. 9 respectively. The magnetic losses in the Y-source converter is sharing 34% of the total losses, this is the double percentage of the magnetic losses in the Z-source converter and 1.5 times the percentage in the boost converter. The capacitor losses in percentages are almost the same in the 3 converters. The switching and conduction losses are the lowest in the boost converter compared to the Z- source and Y-source converters.

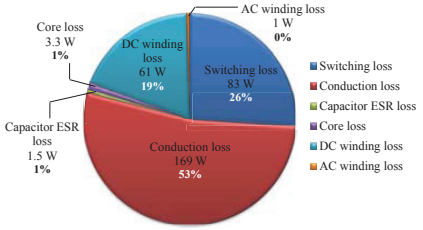

Fig. 7. Distribution of the different losses for the boost converter at 20 kW loading power.

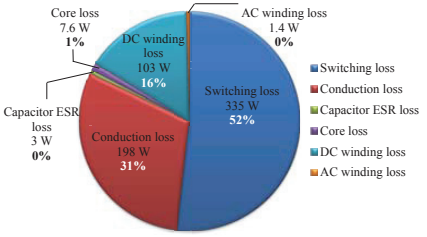

Fig. 8. Distribution of the different losses for the Z-source converter at 20 kW loading power.

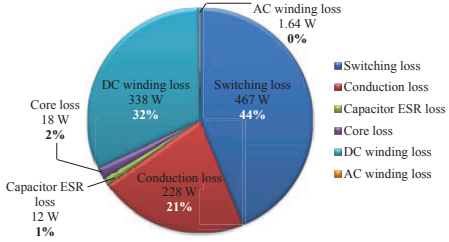

Fig. 9. Distribution of the different losses for the Y-source converter at 20 kW loading power.

V. Conclusions

In this paper a comparison between the Y-source, Z-source and the boost converter has been performed with respect to their thermal behaviour and efficiency. Different loading conditions between 5 kW and 20 kW are considered during the studies on the efficiency and junction temperature of the converters. Investigations on both the magnetic and electrical losses are also given. This paper summarized the comparison between the type of losses at constant loading condition. The thermal performances are quite similar in the 3 converters, and the boost converter is better than both the Z-source and Y-source converters in this specific double voltage gain operation. Different higher voltage gains should be investigated further in the future.

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Loss Distribution and Thermal Behaviour of the Y-source Converter for a Wide Power and Voltage Range

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Loss Distribution and Thermal Behaviour of the Y-source Converter for a Wide Power and Voltage Range

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***Abstract*—The Y-source converter is one of the recent proposed impedance source converters. It has some advantages as having a high voltage gain between the input and output voltage sides using very small duty cycle ratios. For many applications, the input voltage needs to be boosted to higher output voltage, such as for fuel cell, battery electric vehicles and renewable energy applications. Understanding the loss distribution and thermal performance is very important in order to be able to design a reliable converter with longer lifetime. In this paper, the loss distribution of a Y-source converter for a wide voltage and power range is presented. The influence of the heat losses generated in the converter is also considered for different analysis. A simulation model is developed and verified experimentally rated at 300 W.**

I. Introduction

Power converters have been used in many renewable energy applications [1] and more recently with electric vehicles [2] and fuel cell applications [3], which require high voltage gain. Researchers have claimed that impedance source converter has its uniquely advantages such as, having a high voltage gain in the small range of duty cycle and more degree of freedom for setting the voltage gain as needed for a specific application. A collective investigation has been achieved for the Y-source converter [4], [5] and compared with other [6] (conventional boost and Z-source) converters with respect to the thermal and efficiency performances. However, to our knowledge the loss distribution has not been validated experimentally yet.
The Y-source converter circuit diagram and it's two modes of operations are shown in Fig. 1. It is realized by a three-winding coupled inductor (N_1, N_2, and N_3), an active switch SW, two diodes (D_1, D_2), a capacitor C_1 [6], [7]. Due to the discontinuity nature of the current in winding N_1, an input

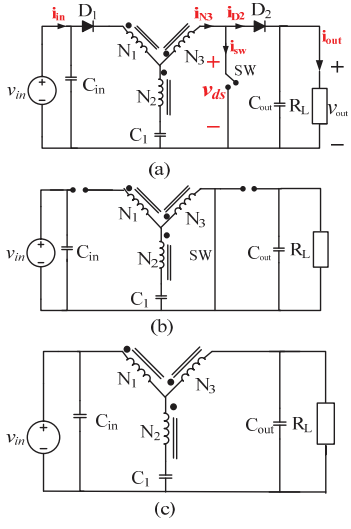
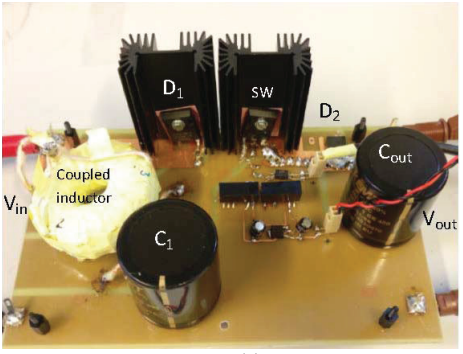
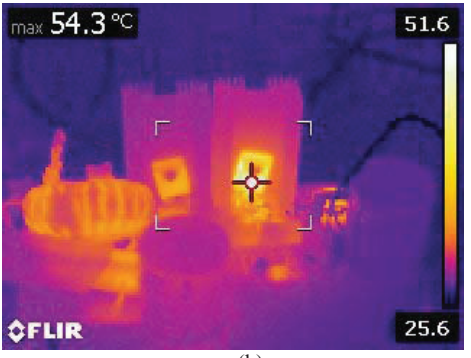


Fig. 1. Boost circuit topology a) Y-source converter equivalent circuit. b) Equivalent circuit for on state. c) Equivalent circuit for off state.



(a)



(b)

Fig. 2. a) Experimental set-up of Y-source converter. b) Thermal image of the prototype Y-source converter operating at nominal load.

capacitor was added in the prototype to smoothen the input current. However, other variations of the Y-source converter which provide a constant input current also exist [8].

II. METHODOLGY

In order to analyse the loss distribution and the efficiency of the converter a prototype of the Y-source converter has been built at 300 W rated power which is shown in Fig. 2(a). The thermal image of the converter shown in Fig. 2(b) reflect the case temperature of all the components in the converter during operation. FLIR thermal camera is used, where it is seen that the highest temperature is of the switch (MOSFET) which indicates a high loss.

In Table I all parameters used in both the simulation model and the prototype design are shown. For the inductor characertics, an MPP core [9] type used, which has the advantage of having lower losses than other types as ferrite cores. Different power loadings are considered for the loss distribution investigation. These losses can be listed as switching, conduction, capacitor ESR, core and winding losses [6] [10].

In Table II the design formulas of the passive elements (inductor and capacitor) are shown.

Furthermore, the thermal performance is also considered, since the junction temperature [11] is an important parameter as it affects the lifetime of the converter. PLECS toolbox is used in the results of the simulation model with different loading powers as shown in Fig. 3.

It is to be noted that the heat losses of the switch and the two diodes also is included in the simulation model in order to investigate the junction temperature.

All analysis are performed under the same operating conditions considering the ambient temperature 25 °C, the switching frequency 20 kHz and the voltage gain (G=4) as listed in Table I.

TABLE I.

Parameters used in the simulation and expermintal prototype of the Y-source converter.

Parameter	Value / description
Rated power (P)	300 W
Voltage gain	4
Winding factor (K) , $K=\frac{N_1+N_3}{N_3-N_2}$	4
Input voltage (V_{in})	60 V
Output voltage (V_{out})	240 V
Duty cycle (d_{st})	0.1875
Turns ratio of coupled inductor (N_1:N_2:N_3)	5:1:3
No. of turns (N_1:N_2:N_3)	80:16:48
Core	MPP C055863A2
Switching frequency (f_s)	20 kHz
Capacitors	C_{in} = 470 µF, 400 V Kemet C_1 = 470 µF, 400 V Kemet C_2 = 470 µF, 400 V Kemet
Switch (Mosfet)	C2M0040120D, 1200v, 60 A
Diode D_1	C3D25170H, 1700v, 26.3 A
Diode D_2	C3D20060D, 600v, 20 A

TABLE II.

Passive component design in the Y-source converter.

Passive Components	Y-source
Inductor	$L_N = A_L N^2 10^{-3}, \quad L_{lik} = \frac{0.292 \times N^{1.056} \times A_c}{L_c}$ $L = L_N + L_{lik}$
Capacitor	$C_1 \geq \frac{D}{2\%(1-D)f_s}\left(\frac{1}{1-k\,D}-1\right)\frac{P_o}{V_o^2}$ $C_{out} = \frac{V_{out} \times D}{R_f \times f_s \times \Delta V_{out}}$

L_N: Nominal inductance, L_{lik}: leakage inductance, K: winding factor

III. EVALUATION OF POWER LOSSES AND THERMAL PERFORMANCE

In this section, all the equations used in calculating the relevant power losses are presented [6], [12]. PLECS toolbox

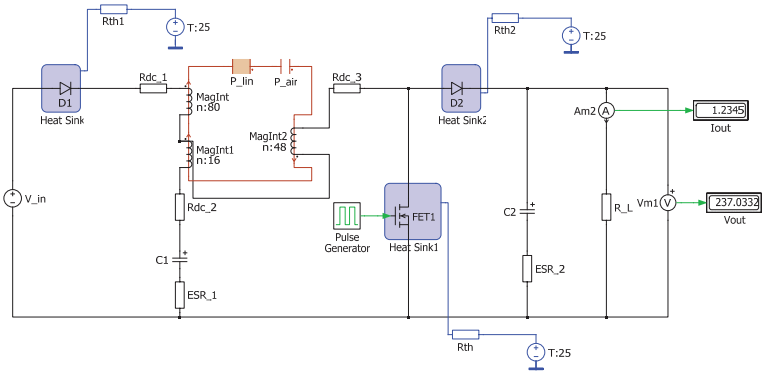


Fig. 3. PLECS model of a Y-source converter for thermal analysis.

is used for the Y-source converter analysis. Loss models are developed in PLECS and compared with the losses equations to map the losses in the simulation model.

A. Switching and conduction losses calculations

1) The MOSFET switching losses are a function of the load current and the switching frequency. The switching losses P_{sw} are expressed in (1) as:

$$P_{SW} = V_{ds} \times I_{sw} \times f_{SW} \times \frac{(Q_{GS2} + Q_{GD})}{I_G} \quad (1)$$

where V_{ds} which is the drain to source voltage, I_{sw} which is the switch (drain) current, f_{sw} is the switching frequency, Q_{GS2} is the gate source charge and Q_{GD} is the gate drain charge, and I_G is the gate current.

2) Conduction losses occur when the device is in full conduction mode. Neither of these losses are a function of the switching frequency.
The conduction losses P_{cond} are expressed in (2) as:

$$P_{cond} = R_{ds(on)} \times I^2_{sw(RMS)} \quad (2)$$

where $R_{ds(on)}$ is the resistance of the selected MOSFET, $I_{sw(RMS)}$ is the root mean square current passing through the MOSFET.

B. Capacitor ESR losses calculations

The Equivalent Series Resistance (ESR) is a parameter, which models the total effect of a large set of energy loss mechanisms in the capacitor occurring under the operating conditions through a certain value of a resistance. So the capacitors ESR losses are expressed in (3) as:

$$P_{cap.loss} = I^2_{cap.} \times ESR \quad (3)$$

where $I_{cap.}$ is the rms current passing through the capacitor, and ESR is the equivalent series resistance measuring the effect of the losses dissipated in the capacitor.

C. Winding and core losses calculations

1) The winding losses are the energy dissipated by the resistance of the wire in the coil. It can be classified into two types of losses (DC and AC winding loss). The DC winding losses can be calculated in (4) as:

$$P_{DC} = I^2_{av} \times R_{DC} \quad (4)$$

where, P_{DC} is the DC copper losses in the winding, I_{av} is the average current passing through the wire, and R_{DC} is the DC resistance of the wire.

2) AC winding losses can be significant for large current ripple and also for high frequency. It can be calculated through the skin effect, where the current density is an exponentially decaying function of the distance into the wire, with a characteristic length δ, which is known as the skin depth.

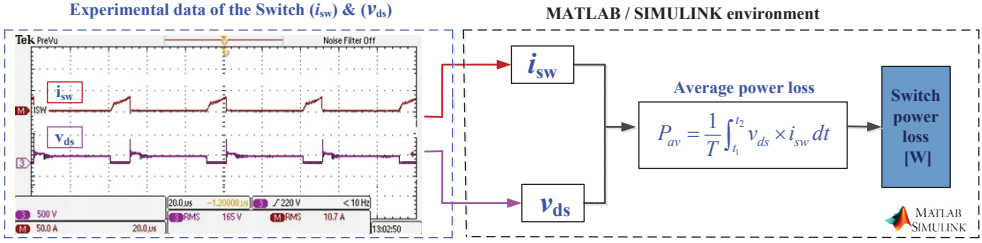


Fig. 4. Illustration diagram of switch loss calculatuion in Y-source converter prototype. a) waveform of the switch current (i_{sw}) and switch volatge (v_{ds}). b) calculation method.

In order to calculate the AC resistance R_{AC}, the thickness h of the wire should be known since it is a function of the DC resistance R_{DC} which can be calculated in (5):

$$R_{AC} = \frac{h}{\delta} \times R_{DC} \tag{5}$$

where, h is the thickness of the wire in cm and δ is the skin depth.
The AC winding losses can be calculated as given in (6):

$$P_{AC} = I_{AC-rms}^2 \times R_{AC} \tag{6}$$

Where, P_{AC} is the AC winding loss, I_{AC-rms} is AC ripple RMS current passing through the wire, and R_{AC} is the AC winding resistance.

3) According to Steinmetz's equation, which is used to calculate the core loss of magnetic materials due to magnetic hysteresis, the core losses is expressed in (7) as:

$$P_v = k f^{\alpha} \hat{B}^{\beta} \tag{7}$$

where $\hat{B}$ is the peak flux density excitation with frequency f, P_v is the time-average power loss per unit volume, and the parameters (α, β, k) are related to the material.

IV. Simulation and Expermintal Results

According to the loss distribution shown in Fig. 5 of the pie chart, and the thermal image shown in Fig. 2(b) the switch (MOSFET) is the most critical component in the Y-source converter as 76% of the total losses are generated from the switch. Therefore, it is decided to focus on validating the switch loss in the prototype.

As stated earlier, the loss calculations in the Y-source simulation model are performed through PLECS toolbox. Since the power losses of the switch could not be measured directly, the total switch loss is calculated based on the switch voltage and current measurements. Therefore, in order to validate the loss calculations in the Y- source prototype converter, the switch voltage (v_{ds}) and current (i_{sw}) waveforms obtained from the prototype are processed in Matlab as shown in Fig. 4.

A. Simulation results

In this section, starting with the initial condition as a dc input voltage source powering the converter where, V_{in}= 60 V and an input capacitor C_{in} is added in order to smoothen the input current signal and at the same time the current passing through the winding N_1, due to the discontinuity nature of the input current i_{in} of the Y-source converter.

Fig. 5 provides more detailed analysis for the amount of losses in the simulated converter at 300 W rated power and four times voltage gain. The results indicate that the switch losses is sharing 76%, the total conduction losses of the two diodes (D_1 and D_2) is 6%, the capacitor loss is 15%, and the heat loss generated from the winding loss is only 3%.

Furthermore, it is noted that reducing the power level from 300 W to 100 W has a significant influence on the loss reduction of the switch.

The results in Fig. 6 shows the losses distribution for the simulated converter at three power levels (100 W, 200 W, and 300 W) and two different voltage gains (3 and 4). The switch losses indicated in this figure are for the total losses (switching and conduction loss) generated from the MOSFET, the diodes loss is the total losses for (D_1 and D_2). In the winding loss, only the DC winding loss is presented since the AC winding loss is minimal so it is neglected. It can be seen from the losses distribution that the losses of the switch is the highest power loss at different power levels and voltage gains.

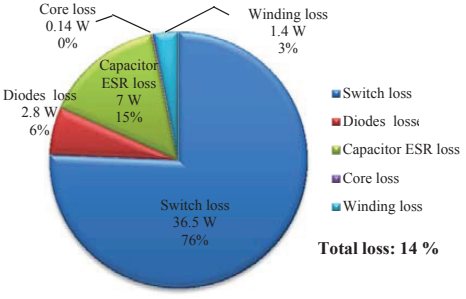


Fig. 5. Simulated power losses distribution for the Y-source converter at 300 W power loading and voltage gain of 4.

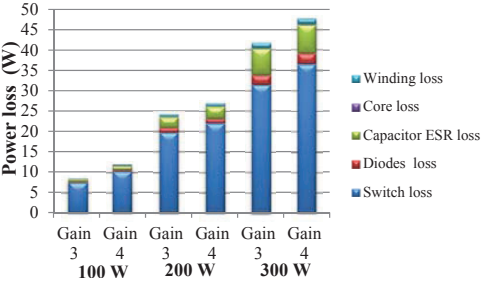


Fig. 6. Simulation results of different losses distribution for the Y-source converter at different loadings 100 W, 200 W and 300 W loading and different voltage gains (3, and 4).

B. Experimental results

The obtained waveforms are captured by a 100 MHz digital phosphor oscilloscope (DPO2014) from Textronix.

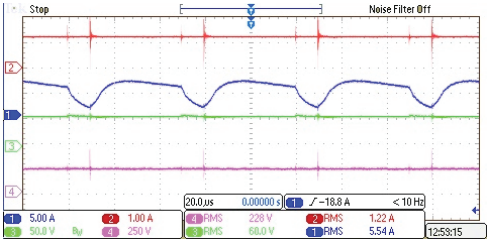


Fig. 7. Experimental waveforms of the Y-source converter with k = 4, d_{st} = 0.19 and P = 300 W at its zoom view where, Ch. 1: input current (i_{in}), Ch. 2: output current (i_{out}), Ch. 3: input voltage (v_{in}), and Ch.4: output voltage (v_{out}).

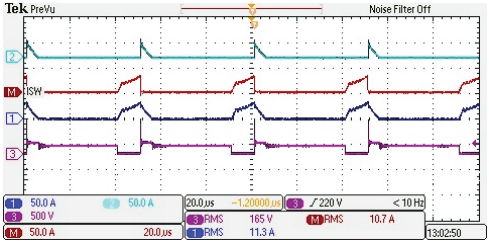


Fig. 8. Experimental waveforms of the Y-source converter with k = 4, d_{st} = 0.19 and P = 300 W at its zoom view Where, Ch. 1: current through winding N_3 , Ch. 2: current through diode D_2 (i_{D_2}), Ch. M: current through SW (i_{sw}) obtained through the math opertaion on the osciliscope, and Ch.3: drain to source voltage (v_{ds}).

In Fig. 7 different experimental currents and voltage waveforms located in the converter are presented where they are as expected under the same conditions as listed in Table I, 300 W rated power and four times gain. The input and output sides are shown ((v_{in}), (i_{in}), (v_{out}) and (i_{out})), where it matches the simulated waveforms.

In order to be able to verify the loss distribution in the Y-source converter, the measurements of the voltage and current passing through each component need to be known. Since the switch loss is the highest generated loss in the converter, two steps are taken for the validation.

First, measuring the general efficacy of the prototype output/input sides. Second, specify closer analysis for the switch losses and its thermal behaviour by including a case/junction temperature measurement.

In the first criteria, the total efficiency of the converter can be measured in both the simulation model and in the prototype from Fig. 7 where the output/input signal can be easily assign the efficiency to be $(P_{out})/(P_{in})$= 84%, while in the simulation model it is equal 86%.

Fig. 8 shows the voltage (v_{ds}) and current (i_{sw}) of the (switch) MOSFET, and the current (i_{D_2}) through diode D_2, and current (i_{N_3}) passing through the winding N_3.

The total switch current can be measured through the math operation in the oscilloscope and compared with simulated one to verify the total switch loss as shown in Fig. 6. The value of the obtained switch current (i_{sw}), which can be seen in Fig. 8 from the prototype, matches with the switch current in the simulation model and as well the same average power loss generated for the total loss of the switch. In the simulation model the total switch loss is 36.5 W, and the measured average power loss from the processed data through Matlab is 38.5 W.

Moreover, the case temperature (54.3°C) of the switch, which can be seen in the thermal image shown in Fig. 2b

matches with the expected calculated value of the simulated junction temperature (62.3°C) while using the same heat sink in both the simulation model and the prototype.

V. CONCLUSION

In this paper an investigation of the Y-source converter has been performed with respect to its thermal behaviour and loss distribution. The results show that the Y-source converter operates with high voltage gain and small duty cycle ratio. It is observed that the Y-source converter experiences high current stress in its switch, which therefore has the highest risk and must be sized appropriately. Loss distribution and case temperature measurement with respect to 300 W power level at the same ambient temperature is performed. Most of the losses in the converter was in the switch. Different power levels have been analyzed and the total power loss of the switch has been verified experimentally. The Y-source converter prototype behaves as expected compared with the simulation model.

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